AD-A017 523

# SEMICONDUCTOR MEASUREMENT TECHNOLOGY: PROGRESS REPORT OCTOBER 1 TO DECEMBER 31, 1974

W. Murray Bullis

National Bureau of Standards

Prepared for:

Defense Nuclear Agency
Advanced Research Project Agency
Strategic Systems Project Office (Navy)

November 1975

NBS-114A (REV. 7-73)

| U.S. DEPT. OF COMM. BIBLIOGRAPHIC DATA SHEET | 1. PUBLICATION OR REPORT NO. NBS Spec. Publ. 400-17 | 2. Gov't Accession No. | 3. Recipient's Accession No. |
|---|---|---|---|

**4. TITLE AND SUBTITLE**

Semiconductor Measurement Technology: Progress Report October 1 to December 31, 1974

**5. Publication Date** November 1975

**6. Performing Organization Code**

**7. AUTHOR(S)** W. Murray Bullis, Editor

**8. Performing Organ. Report No.**

**9. PERFORMING ORGANIZATION NAME AND ADDRESS**

NATIONAL BUREAU OF STANDARDS
DEPARTMENT OF COMMERCE
WASHINGTON, D.C. 20234

**10. Project/Task/Work Unit No.**

**11. Contract/Grant No.** ARPA Order 2347, Pgm. Code 5D10; DNA IACRO 75-816; SSPO Order N0016475P070030, IPR SP6-75-4

**12. Sponsoring Organization Name and Complete Address (Street, City, State, ZIP)**

NBS - Washington, D. C. 20234
ARPA - 1400 Wilson Boulevard, Arlington, Va. 22209
DNA - Washington, D. C. 20305
SSPO - Washington, D. C. 20376

**13. Type of Report & Period Covered** Interim: October 1 to December 31, 1974.

**14. Sponsoring Agency Code**

**16. ABSTRACT** *(A 200-word or less factual summary of most significant information. If document includes a significant bibliography or literature survey, mention it here.)*

This progress report describes NBS activities directed toward the development of methods of measurement for semiconductor materials, process control, and devices. The emphasis is on silicon device technologies. Principal accomplishments during this reporting period include (1) initiation of development of measurement technology for characterizing boron nitride diffusion sources and hydrogen chloride purging gas, (2) application of dc electrical methods with a sensitivity of about 0.1 μm to the measurement of critical dimensions such as the width of diffusion windows, (3) completion of an initial comparison of line-width measurements made with an image shearing eyepiece and a filar eyepiece, and (4) development of procedures for measuring electrically the thermal resistance of the output transistor of integrated Darlington pairs. Also reported are the intermediate results of an interlaboratory evaluation of standard reference wafers for resistivity, evaluation of the deep-depletion method for measuring dopant density with an MOS capacitor, progress on development of mathematical models of dopant profiles, initial results of the reevaluation of Irvin's curve for n-type silicon, analysis of thermally stimulated current and capacitance measurements on MOS capacitors, study of surface carbon contamination which occurs during measurement of silicon by X-ray photoelectron spectroscopy, preliminary measurements of absorbed dose from electron-beam evaporation of aluminum films, initial evaluation of the CCD test structure operating as an MOS capacitor and an MOS transistor, analysis of a TV-microscope system for photomask inspection, initial study of calibration procedures and artifacts for photomask metrology, analysis of the range of applicability of MOS C-V methods for epitaxial layer thickness measurement, use of an optical flying-spot scanner, assessment of damage to selected integrated circuits caused by inspection with a scanning electron microscope, mathematical modeling of ultrasonic bonding, a dry gas method for gross leak testing, and measurements of transistor thermal response. Supplementary data concerning staff, publications, workshops and symposia, standards committee activities, and technical services are also included as appendices.

**17. KEY WORDS** *(six to twelve entries; alphabetical order, capitalize only the first letter of the first key word unless a proper name; separated by semicolons)*

Boron nitride; boron redistribution; capacitance-voltage methods; Darlington pairs; deep depletion; dopant profiles; electrical properties; electron beam evaporator; electron beam induced damage; electronics; epitaxial layer thickness; filar eyepiece; flying-spot scanner; hermeticity; hydrogen chloride gas; image shearing eyepiece; laser interferometry; measurement methods; microelectronics; micrometrology; MOS devices; oxide films; photomask inspection; resistivity; scanning electron microscope; scanning low energy electron probe; semiconductor devices; semiconductor materials; semiconductor process control; silicon; test patterns; thermal resistance; thermal response; thermally stimulated current; ultrasonic bonding; wire bonds; x-ray photoelectron spectroscopy.

**18. AVAILABILITY**

[XX] Unlimited

[ ] For Official Distribution. Do Not Release to NTIS

[XX] Order From Sup. of Doc., U.S. Government Printing Office Washington, D.C. 20402, SD Cat. No. C13.10: 400-17

[X] Order From National Technical Information Service (NTIS) Springfield, Virginia 22151

**19. SECURITY CLASS (THIS REPORT)** UNCLASSIFIED

**21. NO. OF PAGES** 84

**20. SECURITY CLASS (THIS PAGE)** UNCLASSIFIED

**22. Price** $500/225

USCOMM-DC 29042-P74

NBS SPECIAL PUBLICATION 400-17



U.S. DEPARTMENT OF COMMERCE / National Bureau of Standards

# Semiconductor Measurement Technology

## Progress Report

October 1 to December 31, 1974

# NATIONAL BUREAU OF STANDARDS

The National Bureau of Standards[1] was established by an act of Congress March 3, 1901. The Bureau's overall goal is to strengthen and advance the Nation's science and technology and facilitate their effective application for public benefit. To this end, the Bureau conducts research and provides: (1) a basis for the Nation's physical measurement system, (2) scientific and technological services for industry and government, (3) a technical basis for equity in trade, and (4) technical services to promote public safety. The Bureau consists of the Institute for Basic Standards, the Institute for Materials Research, the Institute for Applied Technology, the Institute for Computer Sciences and Technology, and the Office for Information Programs.

**THE INSTITUTE FOR BASIC STANDARDS** provides the central basis within the United States of a complete and consistent system of physical measurement; coordinates that system with measurement systems of other nations; and furnishes essential services leading to accurate and uniform physical measurements throughout the Nation's scientific community, industry, and commerce. The Institute consists of the Office of Measurement Services, the Office of Radiation Measurement and the following Center and divisions:

Applied Mathematics — Electricity — Mechanics — Heat — Optical Physics — Center for Radiation Research: Nuclear Sciences; Applied Radiation — Laboratory Astrophysics[2] — Cryogenics[2] — Electromagnetics[2] — Time and Frequency[2].

**THE INSTITUTE FOR MATERIALS RESEARCH** conducts materials research leading to improved methods of measurement, standards, and data on the properties of well-characterized materials needed by industry, commerce, educational institutions, and Government; provides advisory and research services to other Government agencies; and develops, produces, and distributes standard reference materials. The Institute consists of the Office of Standard Reference Materials, the Office of Air and Water Measurement, and the following divisions:

Analytical Chemistry — Polymers — Metallurgy — Inorganic Materials — Reactor Radiation — Physical Chemistry.

**THE INSTITUTE FOR APPLIED TECHNOLOGY** provides technical services to promote the use of available technology and to facilitate technological innovation in industry and Government; cooperates with public and private organizations leading to the development of technological standards (including mandatory safety standards), codes and methods of test; and provides technical advice and services to Government agencies upon request. The Institute consists of the following divisions and Centers:

Standards Application and Analysis — Electronic Technology — Center for Consumer Product Technology: Product Systems Analysis; Product Engineering — Center for Building Technology; Structures, Materials, and Life Safety; Building Environment; Technical Evaluation and Application — Center for Fire Research: Fire Science; Fire Safety Engineering.

**THE INSTITUTE FOR COMPUTER SCIENCES AND TECHNOLOGY** conducts research and provides technical services designed to aid Government agencies in improving cost effectiveness in the conduct of their programs through the selection, acquisition, and effective utilization of automatic data processing equipment; and serves as the principal focus within the executive branch for the development of Federal standards for automatic data processing equipment, techniques, and computer languages. The Institute consists of the following divisions:

Computer Services — Systems and Software — Computer Systems Engineering — Information Technology.

**THE OFFICE FOR INFORMATION PROGRAMS** promotes optimum dissemination and accessibility of scientific information generated within NBS and other agencies of the Federal Government; promotes the development of the National Standard Reference Data System and a system of information analysis centers dealing with the broader aspects of the National Measurement System; provides appropriate services to ensure that the NBS staff has optimum accessibility to the scientific information of the world. The Office consists of the following organizational units:

Office of Standard Reference Data — Office of Information Activities — Office of Technical Publications — Library — Office of International Relations — Office of International Standards.

---

[1] Headquarters and Laboratories at Gaithersburg, Maryland, unless otherwise noted; mailing address Washington, D.C. 20234.

[2] Located at Boulder, Colorado 80302.

# Semiconductor Measurement Technology
## Progress Report, October 1 to December 31, 1974

W. Murray Bullis, Editor

Electronic Technology Division
Institute for Applied Technology
National Bureau of Standards
Washington, D.C. 20234

Jointly Supported by:
The National Bureau of Standards,
The Defense Nuclear Agency,
The Defense Advanced Research Projects Agency, and
The Navy Strategic Systems Project Office



U.S. DEPARTMENT OF COMMERCE, Rogers C. B. Morton, *Secretary*

James A. Baker, III, *Under Secretary*

Dr. Betsy Ancker-Johnson, *Assistant Secretary for Science and Technology*

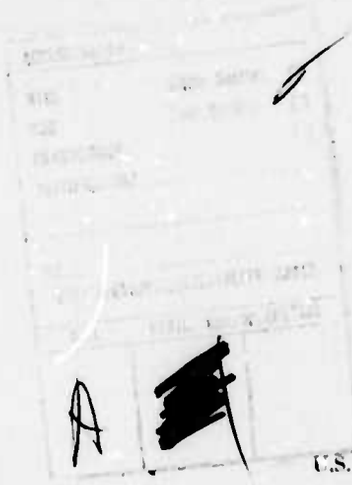
NATIONAL BUREAU OF STANDARDS, Ernest Ambler, *Acting Director*

Issued November 1975

National Bureau of Standards Special Publication 400-17

Nat. Bur. Stand. (U.S.), Spec. Publ. 400-17, 79 pages (Nov. 1975)

CODEN: XNBSAV



U.S. GOVERNMENT PRINTING OFFICE
WASHINGTON: 1975

For sale by the Superintendent of Documents, U.S. Government Printing Office, Washington, D.C. 20402
(Order by SD Catalog No. C13.10:400-17). [redacted]. (Add 25 percent additional for other than U.S. mailing).

# TABLE OF CONTENTS

## SEMICONDUCTOR MEASUREMENT TECHNOLOGY

TABLE OF CONTENTS

# LIST OF FIGURES

LIST OF FIGURES

# LIST OF TABLES

# PREFACE

The Semiconductor Technology Program serves to focus NBS efforts to enhance the performance, interchangeability, and reliability of discrete semiconductor devices and integrated circuits through improvements in measurement technology for use in specifying materials and devices in national and international commerce and for use by industry in controlling device fabrication processes. Its major thrusts are the development of carefully evaluated and well documented test procedures and associated technology and the dissemination of such information to the electronics community. Application of the output by industry will contribute to higher yields, lower cost, and higher reliability of semiconductor devices. The output provides a common basis for the purchase specifications of government agencies which will lead to greater economy in government procurement. In addition, improved measurement technology will provide a basis for controlled improvements in fabrication processes and in essential device characteristics.

The Program receives direct financial support principally from three major sponsors: the Defense Advanced Research Projects Agency (ARPA),* the Defense Nuclear Agency (DNA),† and the National Bureau of Standards (NBS).× In addition, the Program receives support from the U.S. Navy Strategic Systems Project Office.§ The ARPA-supported portion of the Program, Advancement of Reliability, Processing, and Automation for Integrated Circuits with the National Bureau of Standards (ARPA/IC/NBS), addresses critical Defense Department problems in the yield, reliability, and availability of integrated circuits. The DNA-supported portion of the Program emphasizes aspects of the work which relate to radiation response of electron devices for use in military systems. There is considerable overlap between the interests of DNA and ARPA. Measurement oriented activity appropriate to the mission of NBS is a critical element in the achievement of the objectives of both other agencies.

Essential assistance to the Program is also received from the semiconductor industry through cooperative experiments and technical exchanges. NBS interacts with industrial users and suppliers of semiconductor devices through participation in standardizing organizations; through direct consultations with device and material suppliers, government agencies, and other users; and through periodically scheduled symposia and workshops. In addition, progress reports, such as this one, are regularly prepared for issuance in the NBS Special Publication 400 sub-series. More detailed reports such as state-of-the-art reviews, literature compilations, and summaries of technical efforts conducted within the Program are issued as these activities are completed. Reports of this type which are published by NBS also appear in the Special Publication 400 sub-series. Announcements of availability of all publications in this sub-series are sent by the Government Printing Office to those who have requested this service. A request form for this purpose may be found at the end of this report.

---

* Through ARPA Order 2397, Program Code 5D10 (NBS Cost Center 4259555).

† Through Inter-Agency Cost Reimbursement Order 75-816 (NBS Cost Center 4259522).

× Through Scientific and Technical Research Services Cost Centers 4251126, 4252128, and 4254115.

§ Code SP-23, through project order N0016475P070030 administered by Naval Ammunition Depot, Crane, Indiana (NBS Cost Center 4251533) and Code SP-27, through IPR SP6-75-4 (NBS Cost Center 4251547).

# SEMICONDUCTOR MEASUREMENT TECHNOLOGY

PROGRESS REPORT
October 1 to December 31, 1974

*Abstract:* This progress report describes NBS activities directed toward the development of methods of measurement for semiconductor materials, process control, and devices. The emphasis is on silicon device technologies. Principal accomplishments during this reporting period include (1) initiation of development of measurement technology for characterizing boron nitride diffusion sources and hydrogen chloride purging gas, (2) application of dc electrical methods with a sensitivity of about 0.1 μm to the measurement of critical dimensions such as the width of diffusion windows, (3) completion of an initial comparison of line-width measurements made with an image shearing eyepiece and a filar eyepiece, and (4) development of procedures for measuring electrically the thermal resistance of the output transistor of integrated Darlington pairs. Also reported are the intermediate results of an interlaboratory evaluation of standard reference wafers for resistivity, evaluation of the deep-depletion method for measuring dopant density with an MOS capacitor, progress on development of mathematical models of dopant profiles, initial results of the reevaluation of Irvin's curve for n-type silicon, analysis of thermally stimulated current and capacitance measurements on MOS capacitors, study of surface carbon contamination which occurs during measurement of silicon by X-ray photoelectron spectroscopy, preliminary measurements of absorbed dose from electron-beam evaporation of aluminum films, initial evaluation of the CCD test structure operating as an MOS capacitor and an MOS transistor, analysis of a TV-microscope system for photomask inspection, initial study of calibration procedures and artifacts for photomask metrology, analysis of the range of applicability of MOS C-V methods for epitaxial layer thickness measurement, use of an optical flying-spot scanner, assessment of damage to selected integrated circuits caused by inspection with a scanning electron microscope, mathematical modeling of ultrasonic bonding, a dry gas method for gross leak testing, and measurements of transistor thermal response. Supplementary data concerning staff, publications, workshops and symposia, standards committee activities, and technical services are also included as appendices.

*Key Words:* Boron nitride; boron redistribution; capacitance-voltage methods; Darlington pairs; deep depletion; dopant profiles; electrical properties; electron beam evaporator; electron beam induced damage; electronics; epitaxial layer thickness; filar eyepiece; flying-spot scanner; hermeticity; hydrogen chloride gas; image shearing eyepiece; laser interferometry; measurement methods; microelectronics; micrometrology; MOS devices; oxide films; photomask inspection; resistivity; scanning electron microscope; scanning low energy electron probe; semiconductor devices; semiconductor materials; semiconductor process control; silicon; test patterns; thermal resistance; thermal response; thermally stimulated current; ultrasonic bonding; wire bonds; x-ray photoelectron spectroscopy.

# 1. INTRODUCTION

This is a report to the sponsors of the Semiconductor Technology Program on work during the twenty-sixth quarter of the Program. It summarizes work on a wide variety of measurement methods for semiconductor materials, process control, and devices that are being studied at the National Bureau of Standards. The Program, which emphasizes silicon-based device technologies, is a continuing one, and the results and conclusions reported here are subject to modification and refinement.

The work of the Program is divided into a number of tasks, each directed toward the study of a particular material or device property or measurement technique. This report is subdivided according to these tasks. Highlights of activity during the quarter are given in section 2. Subsequent sections deal with each specific task area. References cited are listed in the final section of the report.

The report of each task includes a narrative description of progress made during this reporting period. Additional information concerning the material reported may be obtained directly from individual staff members identified with the task in the report. The organization of the Program staff and telephone numbers are listed in Appendix A.

Background material on the Program and individual tasks may be found in earlier quarterly reports as listed in Appendix B. From time to time, publications are prepared that describe some aspect of the program in greater detail. Current publications of this type are also listed in Appendix B. Reprints or copies of such publications are usually available on request to the author.

Communication with the electronics community is a critical aspect both as input for guidance in planning future program activities and in disseminating the results of the work to potential users. Formal channels for such communication occur in the form of workshops and symposia sponsored or cosponsored by NBS. Currently scheduled seminars and workshops are listed in Appendix C. In addition, the availability of proceedings from past workshops and seminars is indicated in the appendix.

An important part of the work that frequently goes beyond the task structure is participation in the activities of various technical standardizing committees. The list of personnel involved with this work given in Appendix D suggests the extent of this participation. In most cases, details of standardization efforts are reported in connection with the work of a particular task.

Technical services in areas of competence are provided to other NBS activities and other government agencies as they are requested. Usually these are short-term, specialized services that cannot be obtained through normal commercial channels. To indicate the kinds of technology available to the Program, such services provided during the period covered by this report are listed in Appendix E.

# 2. HIGHLIGHTS

Particularly significant accomplishments during this reporting period include (1) initiation of development of measurement technology for characterizing boron nitride diffusion sources and hydrogen chloride purging gas, (2) application of dc electrical methods with a sensitivity of about 0.1 μm to the measurement of critical dimensions such as the width of diffusion windows, (3) completion of an initial comparison of linewidth measurements made with an image-shearing eyepiece and a filar eyepiece, and (4) development of procedures for measuring electrically the thermal resistance of the output transistor of integrated Darlington pairs. Highlights of progress in these and other technical task areas are listed below.

*Process Chemicals Characterization* — Investigations of methods for characterizing selected process chemicals were begun at the Pennsylvania State University with ARPA funding. The initial studies are concentrating on methods for determination of deleterious impurities in boron nitride diffusion sources and water vapor content of hydrogen chloride gas.

*Resistivity; Dopant Profiles* — The interlaboratory evaluation of the long-term precision attainable with silicon standard reference wafers for resistivity measurement by the four-probe method reached its half-way point. Four of the six participating laboratories exhibit good control over their measurements and agreement to much less than 1 percent both with the certified resistivity of the laboratory-owned wafers and with the grand average resistivity of the circulating wafers.

The deep depletion capacitance-voltage characteristic of an MOS capacitor was investigated as a means for determining dopant density of the semiconductor. Four possible sources of error were considered. The deep-depletion method yields a dopant density value more characteristic of the bulk than the more traditional $C_{max} - C_{min}$ method.

A finite difference algorithm was successfully used to solve the moving boundary boron redistribution problem. The solutions for several appropriate sets of conditions were compared with the time independent exact solution to provide a bench mark prior to making calculations for other conditions not amenable to exact solution.

Data were obtained on *n*-type silicon wafers in the resistivity range 0.3 to 5.6 Ω•cm as a beginning to the reevaluation of the relationship between resistivity and free electron density. In this range the data agree closely with the published data of Irvin as fitted by Caughey and Thomas.

*Crystal Defects and Contaminants* — The analysis of the thermally stimulated current and capacitance response of mid-gap acceptor-type defects was extended to the case of an MOS capacitor. The phase I current response was found to yield the same emission temperature as that of a $p^+n$ junction. The sensitivity of the phase II response to various parameters was determined.

*Oxide Film Characterization* — Further study of x-ray photoelectron spectra from the surface of a silicon specimen during various heating cycles confirmed that the carbon film arises from an as yet unidentified residual gas in the spectrometer.

Oxide characterization work has been focussed on the study of techniques for determining and controlling the quality of furnace environments used in growing gate oxides and in subsequent annealing. In conjunction with this effort, a quadrupole mass spectrometer was assembled for measurement of the gas atmosphere in the oxidation furnace, preliminary measurements of sodium contamination in a variety of processing materials were made using flame emission spectroscopy, and steps were taken for determining stability of the oxides produced.

A preliminary measurement was made of the radiation field present during the operation of an electron beam evaporator. During a typical evaporation of an aluminum gate electrode, the gate oxide receives an absorbed dose of the order of 0.1 to $1.8 \times 10^6$ rad($SiO_2$) (0.1 to $1.8 \times 10^4$ J/kg) from the aluminum $K_\alpha$ radiation. An additional dose of approximately similar magnitude arises from the bremsstrahlung continuum.

*Test Patterns* — Evaluation of the test structures on test pattern NBS-3 was begun with detailed investigation of the four base sheet resistors. By combining dc measurements on van der Pauw and bridge structures it was possible to determine the width of the base diffusion window. This technique, which is sensitive to changes in width of about 0.1 μm, utilizes measurements which can be made quickly and at low cost on com-

monly available automatic equipment. The results agreed well with measurements scaled from a photomicrograph.

Other test structures on test pattern NBS-3 are being used in the reevaluation of Irvin's curves. These include the square-array collector resistor, which yielded resistivity values in good agreement with standard four-probe measurements; a circular MOS capacitor over the collector; and a circular base-collector junction.

Initial measurements in the evaluation of the CCD test structure connected as an MOS capacitor or as an MOS field effect transistor were completed.

*Photolithography* — Detailed analyses of various state-of-the-art technologies for automatic inspection of photomasks were begun. The criteria selected were ability to detect a defect of dimension 2 μm and misregistration of ±0.25 μm. The first system analyzed was one composed of a TV camera tube which views the mask through a microscope. It was concluded that inspection of a 3 in. by 3 in. mask in 11 or 12 min would be possible using state-of-the-art components although this is significantly faster than existing prototype of this system.

A polarizing interferometer with 1 nm displacement resolution was constructed for use in making *in situ* measurements of the position of a scanning electron microscope stage. Preliminary measurements using standard stages revealed the need for a more rigid stage assembly with fewer than the usual degrees of freedom for micrometrology experiments.

A preliminary experiment established that it is possible to transfer a line-spacing measurement to a line-width measurement using a multilayer metal artifact in a scanning electron microscope (SEM). The artifact was designed for use in calibrating the magnification of a SEM; it does not simulate the conditions encountered in making dimensional measurements on photomasks. A different artifact was designed with 1 to 10 μm wide lines to simulate the properties of a photomask. This artifact is intended to be fabricated in a film of chromium or iron oxide on an optically flat glass plate.

Comparative measurements of the width of a chromium line on a glass substrate were made using both bright field and dark field illumination and filar and image shearing eyepieces. The measured value was significantly smaller when the filar eyepiece was used with dark field illumination.

*Epitaxial Layer Thickness* — The ramp-voltage and step-relaxation methods for measuring epitaxial layer thickness were analyzed to determine the ranges of thickness and layer resistivity over which they can be used. The ramp-voltage method was found to be applicable over a wider range of parameters.

*Wafer Inspection and Test* — A second laser and improved display amplifiers were added to the flying-spot scanner. Observations were made of a bipolar NAND gate and a C-MOS inverter circuit.

Several typical integrated circuits were studied to assess the damage caused by examination with a scanning electron microscope. No significant damage occurred to a bipolar digital inverter under any condition studied. Both a bipolar linear operational amplifier and a C-MOS inverter exhibited severely degraded characteristics when examined with bias applied, but neither showed significant changes when examined for typical times without bias.

Work continued at the Naval Research Laboratory on the development of an automated scanning low energy electron probe as a non-contacting non-damaging wafer test technique.

*Interconnection Bonding* — Development of the uniform beam model for analysis of the vibration of an ultrasonic bonding tool continued with the addition of a boundary condition to account for the force at the tool tip during the bonding operation. The results suggest that the amplitudes at the unloaded nodal positions and the tool tip can be related to the force during bonding.

Study of the non-destructive accoustic emission test to determine the bond quality of beam lead, flip-chip, or other gang bonded devices continued.

*Hermeticity* — The experimental phase of the interlaboratory evaluation of the radioisotope method for leak testing semiconductor devices was completed. Ten industrial organizations participated in the test.

A rapid gas cycling technique is being evaluated for use as a quantitative, dry gas, gross leak test. Initial calculations suggest that the technique may be suitable for a wide range of leak sizes.

*Thermal Properties of Devices* — Further study confirmed the feasibility of using the modified emitter-only-switching method for measuring the thermal resistance of the output transistor of a monolithic Darlington circuit. It was also found that the voltage between the base of the input transistor and the emitter of the output transistor, measured during the power-off portion of the thermal resistance measuring cycle, is a good indicator of the onset of a current constriction in the output transistor.

Development of electrical techniques for estimating peak junction temperature of power transistors continued. It was established that one of the necessary quantities, the total active area of the device, can be determined from measurements of the heating response of the device.

Work was initiated on an automatic stepping stage for use with the infrared microradiometer in order to facilitate measurement of surface temperature distributions on power devices and integrated circuits.

Recommendations concerning changes to the thermal resistance methods in MIL-STD-750B, for discrete semiconductor devices, were formulated at the request of EIA Committee G-12 on Solid State Devices. These recommendations, which are based on standards developed by various EIA-JEDEC Committees and draw heavily on prior NBS work, were submitted to the Defense Electronics Supply Center for consideration.

# 3. PROCESS CHEMICALS CHARACTERIZATION

## 3.1. Introduction

An important factor for the improvement of process control and reliability of digital integrated circuits is the need to control the purity of the various chemicals used during the fabrication process. In many cases these chemicals, such as diffusion sources, epitaxy chemicals, and other chemicals are supplied by vendors with little or no insight into the material purity levels that are detrimental to device reliability and performance. This is particularly true since normal chemical analysis techniques which might be used by suppliers do not provide the necessary detectability limits. Often only the electrical testing of the final device structure brings out the influence a particular chemical impurity has on device performance and in the case of integrated circuits it is generally impossible to gain access to individual devices which make up the circuit.

A new effort has been undertaken at the Solid State Device Laboratory of Pennsylvania State University in order to develop measurement techniques for monitoring chemicals used in digital integrated circuit manufacturing. The study is aimed at chemicals used in the three principal processes of oxidation, diffusion, and epitaxy. It is intended to analyze various chemicals, then use these chemicals to process devices or test patterns which can be analyzed by electrical tests. An important aspect of the initial phase effort is the determination of the detectability limits of the analytical and electrical measurements and degree of correlation of electrical measurement techniques with analytical measurements.

In the initial investigations the materials to be characterized with respect to their impurity levels are boron nitride, compositions of boron nitride with silica, and hydrogen chloride gas. These materials were selected because of their wide use in diffusion and oxidation processes in digital integrated circuit fabrication. Boron nitride wafers have gained acceptance as diffusion sources as silicon wafer diameters have increased [1]. The use of hydrogen chloride gas has recently gained wide acceptance in the growth of high quality oxides particularly in MOS technology.

Boron nitride has evolved from a refractory material to one used in semiconductor applications. Because of its original refractory nature, the material has metallic impurities, in the 1 to 100 ppm levels, which can lead to reduced carrier lifetime and high reverse currents in $p$-$n$ junctions. The present study seeks to determine the tolerable level of these metallic impurities in boron nitride diffusion sources. Experiments using emission spectroscopy, will be conducted to determine the density at levels of 0.5 ppm or greater of impurities, such as gold, iron, or copper, in the boron nitride as manufactured. Next the boron oxide glass transferred to the silicon wafer during diffusion will be analyzed using flameless atomic absorption, at levels of 1 ppm or less, to determine how much of the impurity has been transferred. Then thermally stimulated current and carrier lifetime measurements will be made to determine the level and energies of impurities that are present in $p$-$n$ junctions fabricated using the boron nitride source.

These experiments will provide the necessary correlation data needed to establish chemical purity standards and feedback to boron nitride manufacturers. Boron nitride wafers and powder which have been manufactured by different techniques will be furnished by a cooperating supplier during the course of the study.

The study of hydrogen chloride gas is focussed on the determination of the allowable water vapor level. Studies have shown that the presence of small amounts of water vapor can destroy the passivation effects of hydrogen chloride [2]. Oxide layers will be grown and examined for various levels of water vapor in the hydrogen chloride. Dynamic growth rates as a function of time will be measured for different levels of water vapor using thermogravimetric analysis which has a detectability limit of 5 nm of silicon dioxide. The hydrogen chloride and water vapor mixtures will be furnished by a second cooperating supplier. (J. Stach*)

---

* Work conducted at the Pennsylvania State University under NBS contract 5-35717. NBS contact for additional technical information: R. I. Scace.

## 3.2. Boron Nitride

Prints of the mask set for test pattern NBS-2 (NBS Tech. Note 788, pp. 15-17) [3] have been obtained and a process developed to enable the fabrication of boron nitride diffused diodes and gated MOS capacitors for use in the study of boron nitride diffusion sources. The electrical measurement methods that are being emphasized initially include thermally and optically stimulated techniques [4] and carrier lifetime. Mechanical, electrical, and optical designs for the system to make measurements of thermally and optically stimulated current and capacitance were completed and the parts are being assembled. The system for measuring carrier lifetime by the MOS capacitance method [5] has also been designed.

The analysis of various boron nitride starting powders and the development of suitable standards for emission spectroscopy measurements are currently being undertaken. A joint effort with the supplier has been initiated to determine the impurity levels introduced during various stages of boron nitride wafer fabrication in typical production runs. This lot of wafers (100% boron nitride and boron nitride/silicon dioxide) is then to be used to study impurity partitioning during activation (surface oxidation of the boron nitride to boron oxide) and diffusion. (J. Stach*)

## 3.3. Hydrogen Chloride

The design of the system for thermogravimetric analysis has been completed. This includes thermal, gas handling, and specimen fixtures. Arrangements have been made with the cooperating manufacturer to supply various samples of hydrogen chloride for thermogravimetric analysis. Controlled amounts of water vapor will be introduced from a special moisture mixture supplied by the manufacturer. (J. Stach*)

# 4. RESISTIVITY; DOPANT PROFILES

## 4.1. Standard Reference Materials

In conjunction with offering for sale standard reference silicon wafers with certified resistivity values for use with four-probe measurements [6], NBS is conducting a multipass experiment with five other laboratories to test the long-term precision attainable with these wafers and to determine their stability. The experiment requires each laboratory to measure monthly its own set of standard reference wafers according to ASTM Method F 84 [7] with the exception that only two resistivity values instead of the normal ten be measured for each wafer. Two additional sets of standard reference wafers are being circulated to the participating laboratories such that each month one of the laboratories also measures these circulating wafers according to the same method except that five measurements are made on each circulating wafer. The circulating wafers have been to each laboratory once which brings the experiment approximately to its half-way point although some laboratories have reported more measurements than others on the non-circulating wafers.

The results of this first phase of the experiment are summarized in table 1. With two exceptions, the participants appear to have good control over the measurements. Laboratory 2 shows a significant high-side bias on its high-resistivity wafer as well as the greatest variability in measurements of in-house wafers. Laboratory 4 shows a strong high-side bias in all of its measurements despite the good reproducibility of these measurements. The test will be concluded after each laboratory reports 12 sets of measurements on its in-house wafers and after the circulating wafers complete their second cycle. (F. H. Brewer)

## 4.2. Dynamic MOS C-V Method

In the traditional high frequency MOS capacitance-voltage (C-V) measurement (NBS Spec. Publ. 400-4, pp. 37-38), the rate of the voltage bias sweep is kept slow enough to allow equilibrium in the inversion regime to be maintained through minority carrier generation. As a result, the semiconductor space charge region assumes a fixed width and the MOS capacitance saturates to its minimum value, shown in figure 1 as $C_{min}$. If however, the sweep rate is rapid enough that the minority carrier generation is insufficient to maintain equilibrium, the semiconductor becomes depleted and the space charge width increases. The capacitance associated with this depletion regime is shown as curve $C_D$ in figure 1. The dopant density profile can be deduced from this C-V characteristic when it is analyzed according to standard models [8].

In the experiment, the bias applied to the MOS capacitor is a repetitive (approximately 10 Hz) ramp or triangular voltage of the appropriate magnitude and polarity. A three-terminal capacitance bridge provides an analog signal proportional to the measured capacitance. Both the analog capacitance signal and the applied ramp voltage are simultaneously displayed on a dual channel oscilloscope. Typical waveforms are shown in figure 2 as they appear on the oscilloscope face. The data acquisition and analysis system employed permits processing of the data displayed on the oscilloscope.

The algorithm for the calculation is based on the expression for the dopant density, N(X), at the edge of the space charge region as deduced from the simple depletion model [8]:

$$N(X) = \frac{2}{qK_s\varepsilon_0}\left(\frac{dC^{-2}}{dV}\right)^{-1}, \qquad (1)$$

where X is the depletion width, q is the electronic charge, $K_s$ is the relative dielectric constant of silicon, $\varepsilon_0$ is the permittivity of free space, C is the measured capacitance per unit area, and V is the bias voltage. Under software control the C(t) and V(t) waveforms are sampled and stored; typically 1000 scans are averaged to produce a smooth curve. Time is used as an independent parameter to find the derivative in eq (1). From the smoothed capacitance curve, the quantity $[C(t)]^{-2}$ is calculated and differentiated to obtain $d[C(t)]^{-2}/dt$. Similarly the smoothed voltage curve is differentiated to find dV/dt. The depletion width corresponding to each value of bias voltage is calculated from

$$X = K_s\varepsilon_0\left(\frac{1}{C} - \frac{1}{C_o}\right), \qquad (2)$$

where $C_o$ is the oxide capacitance per unit area and C is the measured capacitance per unit area for the particular voltage.

Table 1 - Intermediate Results of Interlaboratory Test on SRM 1520

a. Laboratory-Owned Wafers with Nominal Resistivity of 0.1 Ω·cm

| Laboratory Reporting | Certified Resistivity, Ω·cm | Number of Measurement Pairs Reported | Average Resistivity, Ω·cm | Sample Std. Dev., % |
|---|---|---|---|---|
| 1 | 0.11974 | 8 | 0.12006 | 0.21 |
| 2 | 0.11825 | 6 | 0.11883 | 1.24 |
| 3 | 0.11885 | 5 | 0.11937 | 0.58 |
| 4 | 0.12033 | 5 | 0.12261 | 0.66 |
| 5 | 0.11925 | 8 | 0.11849 | 1.03 |
| 6 | 0.12056 | 6 | 0.11994 | 0.49 |

b. Laboratory-Owned Wafers with Nominal Resistivity of 10 Ω·cm

| Laboratory Reporting | Certified Resistivity, Ω·cm | Number of Measurement Pairs Reported | Average Resistivity, Ω·cm | Sample Std. Dev., % |
|---|---|---|---|---|
| 1 | 11.251 | 8 | 11.309 | 0.27 |
| 2 | 11.118 | 6 | 11.351 | 1.65 |
| 3 | 11.178 | 5 | 11.246 | 0.58 |
| 4 | 11.098 | 5 | 11.406 | 0.40 |
| 5 | 11.062 | 8 | 11.078 | 1.23 |
| 6 | 11.054 | 6 | 11.081 | 0.48 |

c. Circulating Wafers with Nominal Resistivity of 0.1 Ω·cm

| | Wafer A-13 | | Wafer A-17 | |
|---|---|---|---|---|
| Laboratory Reporting | Average Resistivity, Ω·cm | Sample Std. Dev., % | Average Resistivity, Ω·cm | Sample Std. Dev., % |
| Reference[a] | 0.1194 | | 0.1200 | |
| 1 | 0.1192 | 0.40 | 0.1198 | 0.13 |
| 2 | 0.1194 | 0.2 | 0.1197 | 0.1 |
| 3 | 0.1190 | 0.15 | 0.1197 | 0.37 |
| 4 | 0.1223 | 0.04 | 0.1240 | 0.36 |
| 5 | 0.1196 | 0.21 | 0.1201 | 0.19 |
| 6 | 0.1183 | 0.21 | 0.1191 | 0.31 |
| Average[b] | 0.11963 | 1.15 | 0.12040 | 1.49 |

d. Circulating Wafers with Nominal Resistivity of 10 Ω·cm

| | Wafer B-84 | | Wafer A-17 | |
|---|---|---|---|---|
| Laboratory Reporting | Average Resistivity, Ω·cm | Sample Std. Dev., % | Average Resistivity, Ω·cm | Sample Std. Dev., % |
| Reference[a] | 11.11 | | 11.20 | |
| 1 | 11.11 | 0.13 | 11.18 | 0.16 |
| 2 | 11.05 | 0.6 | 11.07 | 0.9 |
| 3 | 11.14 | 0.44 | 11.26 | 0.59 |
| 4 | 11.39 | 0.39 | 11.47 | 0.21 |
| 5 | 11.17 | 0.10 | 11.25 | 0.11 |
| 6 | 11.05 | 0.13 | 11.10 | 0.31 |
| Average[b] | 11.15 | 1.13 | 11.22 | 1.28 |

[a]The reference value was obtained from the overall average of two sets of readings by each of two operators at NBS taken over a period of two weeks.

[b]Mean and sample standard deviation of the individual laboratory averages.

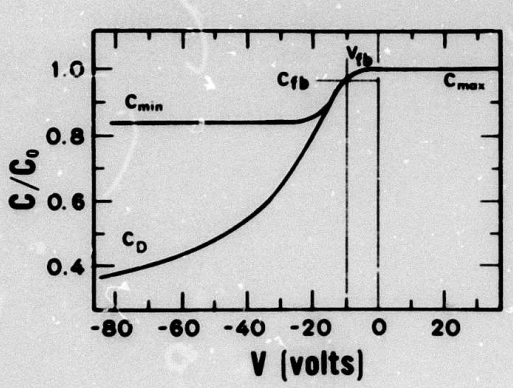



Figure 1. Experimental equilibrium and non-equilibrium high frequency capacitance-voltage characteristics of an *n*-type MOS capacitor. ($C_{max}$ = 7.54 pF; oxide thickness = 522 nm; the flat-band capacitance, $C_{fb}$, occurs at the flat-band voltage, $V_{fb}$.)

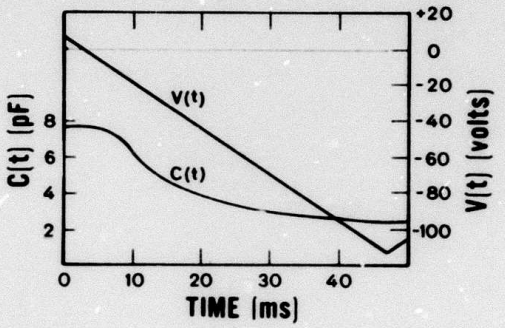



Figure 2. Experimental oscilloscope traces of voltage, V(t), and non-equilibrium capacitance, C(t), as a function of time for an *n*-type MOS capacitor.

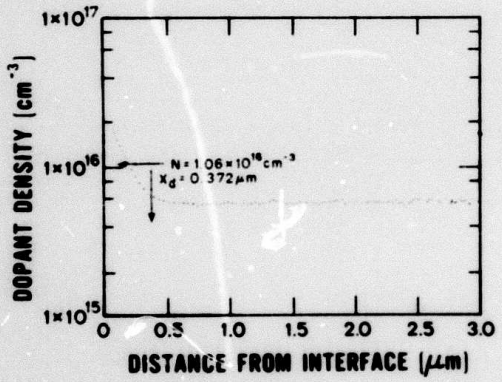



Figure 3. Dopant profile calculated from non-equilibrium (deep depletion) capacitance-voltage characteristics.

Results of a typical measurement are shown in figure 3 as a plot of dopant density against distance from the silicon-oxide interface. The specimen used was phosphorus-doped with a nominal resistivity of 1 Ω·cm. The wet oxide, grown at 1000°C for 150 min, had a nominal thickness of 500 nm. The aluminum gate electrodes were evaporated with an electron-beam evaporator and the wafer was annealed in nitrogen for 30 min at 500°C.

There are at least four sources of error in the profile which must be considered. First, at large depletion depths the C(t) curve is changing very slowly. The differentiation in this region is then very sensitive to random fluctuations in the C(t) curve; as a result there is likely to be appreciable scatter in the calculated dopant density at large distances from the interface, as can be seen in figure 3. Some improvement could be made by averaging over longer periods of time or by using a larger differentiation grid as the change in capacitance becomes small.

A second source of error is the effect of fringing fields on the MOS capacitor. For materials of relatively low dopant density ($\sim 10^{14}$ cm$^{-3}$) depletion depths can be large ($\sim$ 10 μm). This causes a spreading of the electric fields away from the gate and could cause an increase in the measured capacitance. This edge effect is serious for devices where the maximum depletion depth is a finite fraction of the device radius. Typically, the presence of fringing fields causes the calculated dopant density to be larger than the actual dopant density; the error increases as the depletion depth increases.

The third source of error arises because of limitations in the simple depletion model. In the ideal case, depletion starts at the flat-band voltage. Experimentally, the capacitance near the flat-band voltage is always less than the theoretical depletion capacitance. Therefore, the calculated profile lies above the true profile near the flat-band condition until the true depletion regime is entered. In the example shown in figure 3, the first data point on the left corresponds to a voltage slightly more negative than the flat-band voltage so this error may be present.

The fourth source of error arises from the departure of the C-V characteristic from the ideal as a result of fast interface states. Interface states contribute to the capacitance and will cause distortion or structure in the calculated profile. When present they exert their greatest influence in the surface region of the profile.

One other point to be considered is the comparison of the dopant density as determined by the traditional $C_{max} - C_{min}$ method (NBS Spec. Publ. 400-4, pp. 37-38) and that determined by the deep depletion method described here. The dopant density determined by the $C_{max} - C_{min}$ method is the average density within the equilibrium depletion depth. In figure 3 the horizontal and vertical arrows indicate the dopant density (N) and the equilibrium depletion depth ($X_d$) determined from this method. Note that the calculated density is significantly higher than the bulk density determined from the deep depletion technique which allows penetration of the space charge region much farther than the equilibrium high frequency technique which is employed in the $C_{max} - C_{min}$ method. It is clear that the $C_{max} - C_{min}$ technique determines a dopant density which is more characteristic of the surface region and may have little relation to the bulk dopant density. (S. T. Hsu)

## 4.3. Mathematical Models of Dopant Profiles

This report outlines a finite difference algorithm [9] for the solution of the boron redistribution problem described previously (NBS Spec. Publs. 400-1, pp. 9-11, and 400-4, pp. 9-11). This algorithm consists of a set of algebraic equations whose solution approximates the solution of the partial differential equations which govern the boron concentration in the silicon and the silicon dioxide (NBS Spec. Publ. 400-1, eqs (4), (5), and (7), pp. 10-11).

As previously discussed two coordinate systems are used: in the silicon, a fixed system with its origin at the initial silicon surface, and in the oxide, a system with its origin at the oxide-air interface which moves away from the initial silicon surface with a velocity inversely proportional to the square root of the time. The silicon-oxide interface moves in the opposite direction with a similar velocity. The motion of this interface complicates the

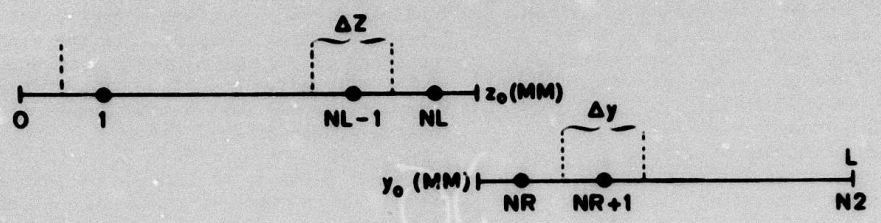



Figure 4. Finite difference grid used in solving boron redistribution problem.

Table 2 - Boron Concentration in Silicon at the Moving Boundary between the Silicon and Silicon Dioxide

| Case | m | $C_s$[a] | $C_b$[a] | $C_2(y_0(t))$[a,b] | $\Delta t$[a] | k | $z_0(k\Delta t)$ | $CB(2,z_0(k\Delta t))$[a] |
|---|---|---|---|---|---|---|---|---|
| 1a | 1.2 | 0.1 | 10 | 4.466 | 90 | 49 | 0.067 | 4.594 |
| b | | | | | 800 | 49 | 0.1988 | 4.594 |
| 2a | 1.2 | 10 | 10 | 9.653 | 90 | 49 | 0.0669 | 9.558 |
| b | | | | | 800 | 49 | 0.1988 | 9.557 |
| 3a | 1.2 | 0.1 | 10 | 6.187 | 800 | 1 | | 8.82 |
| b | | | | | 800 | 5 | | 7.122 |
| c | | | | | 800 | 49 | | 6.386 |
| 4a | 0.5 | 0.1 | 10 | 2.264 | 800 | 1 | | 4.718 |
| b | | | | | 800 | 4 | | 2.719 |
| c | | | | | 800 | 97 | | 2.281 |

[a]Arbitrary units.

[b]Calculated from analytic solution, ref. 11.

application of the finite difference technique. The grid used is depicted in figure 4. The mesh width $\Delta t$ in the time domain and the mesh widths $\Delta y$ and $\Delta z$ in the silicon and the oxide respectively are coupled. In the oxide there are NL interior grid points (1, 2, ..., NL-1, NL) separated by $\Delta z$. The position of the interface at the time $(MM)\Delta t$ is denoted by $z_o(MM)$, where MM is the number of time intervals since the beginning of the oxidation; the distance between $(NL)\Delta z$ and $z_o(MM)$ varies. In the silicon the first full mesh width to the right of the interface $y_o(MM)$ begins at $(NR)\Delta y$; the interior grid points (NR, NR+1, ..., N2), spaced $\Delta y$ apart, extend to $(N2)\Delta y$.

In the oxide the approximate solution has the form $C_1(n_1\Delta z, k\Delta t)$ for $1 < n_1 \leq NL$ and $k \geq 0$ at the grid points and $CB(1, z_o(k\Delta t))$ for $k \geq 0$ at the boundary. In the silicon the approximate solution has the form $C_2(n_2\Delta y, k\Delta t)$ for $NR \leq n_2 \leq N2$ and $k \geq 0$ at the grid points and $CB(2, y_o(k\Delta t))$ for $k \geq 0$ at the boundary.

The algebraic equations which comprise the finite difference equations are obtained by discretizing the integral-conservation equivalents of the above mentioned partial differential equations. In particular, the differential form of the conservation of mass at the boundary, expressed in integral form is

$$\frac{d}{dt}\left[\int_{Z_A}^{Z_o(t)} C_1(z,t)dz + \int_{Y_o(t)}^{Y_B} C_2(y,t)dy\right]$$

$$= -D_1 \frac{\partial}{\partial z} C_1(Z_A,t) + D_2 \frac{\partial}{\partial y} C_2(Y_B,t), \qquad (3)$$

where $Z_A \equiv (NL)\Delta z$ and $Y_B \equiv (NR)\Delta y$. By approximating the derivatives in eq (3) by their finite difference equivalents and the integrals by quadratures, one obtains an implicit algebraic equation of the form

$$A \cdot C_1(NL, MM) + B \cdot CB(1, MM)$$

$$+ C \cdot C_2(NR, MM) + D \cdot CB(2, MM) = F, \qquad (4)$$

where the coefficients A, B, C, D, and F are constants related to the grid approximation. This equation and the boundary condition (NBS Spec. Publ. 400-1, eq (6), pp. 10-11)

$$CB(2, MM) = mCB(1, MM),$$

where m is the segregation coefficient, represent two equations in the unknown boundary values CB(1, MM) and CB(2, MM). These equations and the usual implicit equations associated with all the interior grid points form a linear algebraic system which can be solved by a variant of the well known method for treating tridiagonal systems [10]. To provide a bench mark comparison, this system was solved for several cases under conditions for which the analytic solution of Grove *et al.* [11] can be obtained. Table 2 lists a comparison between these solutions. If the segregation coefficient is substantially different from one, the value $CB(2, z_o(k\Delta t))$ calculated for a very short time after the oxidation begins is much larger than the value $C_2(y_o(t))$ calculated from the analytic solution. This is not unexpected since $C_2(y_o(t))$, which is independent of time, is not equal to $C_b$. Hence $C_2(y_o(t),t)$ is discontinuous at time zero. The total time taken for the approximate solution to reach its steady state value depends on the time step employed; this time is shorter if the time step is smaller.

(S. R. Kraft* and M. G. Buehler)

## 4.4. Reevaluation of Irvin's Curves

Detailed experimental redetermination of the relationships between resistivity and dopant density in silicon (NBS Spec. Publ. 400-4, p. 13) was begun. The relationships as reported by Irvin [12] are in wide use throughout the industry; the graphical forms of these relationships are commonly known as Irvin's curves.

Preliminary data were obtained using appropriate test structures of Test Pattern NBS-3 (NBS Spec. Publ. 400-12, pp. 19-22) fabricated in three wafers of *n*-type (phosphorus doped) silicon. Bulk resistivity of the original *n*-type portion of the wafers was determined from measurements on structure 3.17, the collector four-probe resistor (sec. 7.3), corrected to 300 K [13]. Free carrier density was determined from measurements on structure 3.8, MOS capacitor over collector (sec. 7.4), or on structure

*NBS Mathematical Analysis Section, Applied Mathematics Division.

3.10, base-collector diode (sec. 7.5). The results of these measurements are summarized in table 3.

The measurements made on the collector four-probe resistor were very repeatable on a given device. The data reported in the table are averages for several devices in the same general area on the wafer.

The carrier density values from the MOS capacitor were determined by the deep depletion method (sec. 6.3). These values have an estimated uncertainty of ±5 percent. The base-collector diode is located a little over 1 mm away from the MOS capacitor. Carrier density values were determined from the diode by the junction capacitance-voltage (C-V) method (NBS Tech. Note 788, pp. 9-11). A set of carrier density values from a diode had an average standard deviation of less than 1 percent. Because of the strong dependence of the calculated carrier density on the area of the base diffusion, the diameter of the diffusion for this processing run was measured by photomicrographic procedures and found equal to the nominal value (432 μm) within 1 μm.

The carrier density values from the junction C-V method were used for computing the mobility as this method is considered to be better characterized than the MOS procedure at this time. The mobility value calculated for each wafer is based on the average value of resistivity and carrier density. The mobility values for these wafers are about 5 percent larger than those calculated by the equation of Caughey and Thomas [14] which closely fits Irvin's curve for $n$-type silicon. However, these preliminary results suggest that the mobility calculated from the Caughey-Thomas equation agrees with the experimentally determined value within the estimated errors in the resistivity range studied. (W. R. Thurber, R. L. Mattis, R. Y. Koyama, Y. M. Liu, and M. G. Buehler)

Table 3 - Preliminary Resistivity-Carrier Density Data for Phosphorus-Doped Silicon at 300 K

| Slice No. | A0.27Ph-1 | A1.0Ph-1 | 5200 |
|---|---|---|---|
| $\rho$, Ω·cm | 0.299±0.015 | 1.035±0.005 | 5.59±0.21 |
| n, $cm^{-3}$(MOS) | $(2.12\pm0.19) \times 10^{16}$ | $(4.76\pm0.20) \times 10^{15}$ | $8.34 \times 10^{14}$[b] |
| n, $cm^{-3}$(jcn) | $(2.00\pm0.03) \times 10^{16}$ | $(4.82\pm0.13) \times 10^{15}$ | $8.20 \times 10^{14}$[b] |
| $\bar{\mu}$, $cm^2/V\cdot s$(exp) | 1044±55 | 1251±34 | 1362 |
| $\mu$, $cm^2/V\cdot s$(calc) | 1000 | 1188 | 1287 |
| % diff[a] | 4.4 | 5.3 | 5.8 |

[a] $[\bar{\mu}(exp) - \mu(calc)]/\mu(calc)$

[b] single device

# 5. CRYSTAL DEFECTS AND CONTAMINANTS

## 5.1. Thermally Stimulated Current and Capacitance Measurements

Analysis of thermally stimulated current and capacitance measurements continued with emphasis on the thermally stimulated current response from the gold acceptor in an $n$-type silicon MOS capacitor. For the analysis, it was assumed that only those defects between $W_{IIf}$, the steady state inversion width and the depletion width at the end of phase II of the dynathermal response measurement (NBS Spec. Publ. 400-1, pp. 16-19), and $W_{Ii}$, the depletion width at the start of the dynathermal response are initially charged and that defects between the oxide-silicon interface and $W_{IIf}$ are uncharged. In order to achieve this condition, the MOS capacitor is cooled to low temperatures with the depletion width held at $W_{IIf}$ by applying a bias voltage sufficient to drive the capacitor into the inversion region; once the low temperature is reached, a larger bias which widens the depletion width to $W_{Ii}$ is applied.

Detailed calculations were carried out with procedures analogous to those used previously in analyzing a $p^+n$ junction (NBS Spec. Publ. 400-12, pp. 8-11).* The phase I current response of the MOS capacitor was found to be somewhat less than that of a $p^+n$ junction with the same values of donor density, $N_d$, and gold density, $N_t$, biased so that the portion of the depletion width in which the defects are not charged is the same. However, under such similar bias conditions the current response of the MOS capacitor is related to that of the $p^+n$ junction in such a way that the maximum in the dynathermal current response occurs at the same temperature, $T_{Ie}$, for both structures.

The phase II current response of an MOS capacitor depends on the heating rate, $\beta$, the ratio $N_d/N_t$, the ratio $H = W_{IIf}/W_{Ii}$, and a geometrical parameter $G = \varepsilon_o W_{IIf}/\varepsilon_s X_o$ where $\varepsilon_s$ is the dielectric constant of silicon, $\varepsilon_o$ is the dielectric constant of silicon dioxide, and $X_o$ is the oxide thickness.

The sensitivity of the phase II current response to these parameters was studied assuming that the temperature is raised slowly enough that steady state conditions prevail (NBS Spec. Publ. 400-8, p. 32).

The parameters were varied one at a time over the following ranges:

$$0.2\ \text{K/s} \leq \beta \leq 10\ \text{K/s}$$
$$5 \leq N_d/N_t \leq 100$$
$$0.1 \leq H \leq 0.9$$
$$0.1 \leq G \leq 10$$

When not being varied the parameters were held at $\beta = 10$ K/s, $N_d/N_t = 100$, $H = 0.2$, and $G = 1$. The individual results are shown in figures 5-8. As shown in figure 5, an increase in the heating rate causes $T_{IIe}$, the temperature of the current maximum, to increase. This is the same behavior as that observed for the phase I current peak $T_{Ie}$. As shown in figure 6, a decrease in the density of generation sites $N_t$ relative to the background dopant density $N_d$, causes $T_{IIe}$ to increase, for it takes higher temperatures (higher hole emission rates) to satisfy the inversion conditions at the oxide-silicon interface. Likewise, as shown in figure 7, reduction of the number of generation sites by restriction of the initial depletion width (increasing H) causes $T_{IIe}$ to increase. Finally, as shown in figure 8, a decrease in the oxide thickness relative to $W_{IIf}$ (an increase in G) also results in an increase in $T_{IIe}$.

The relationship between $T_{IIe}$ and heating rate scaled by the factor F previously discussed (NBS Spec. Publ. 400-4, p. 33) was shown to be independent of these parameters over all ranges except for $N_d/N_t < 20$. It was also shown that for all values of H, F can be determined from measurable capacitances:

$$F = \frac{C_{IIf}C_{IIe}(C_{IIf}C_o - C_{IIe}^2)(C_{If}^2 - C_{Ii}^2)}{C_o C_{If}^2 (C_o - C_{IIe})(C_{IIf}^2 - C_{Ii}^2)} \quad (5)$$

where the capacitances are identified in figure 9 which shows the dynathermal current and capacitance response of an ideal, gold-doped $n$-type MOS capacitor.

---

* The complete analysis, summarized here, is being prepared for publication as a separate report.

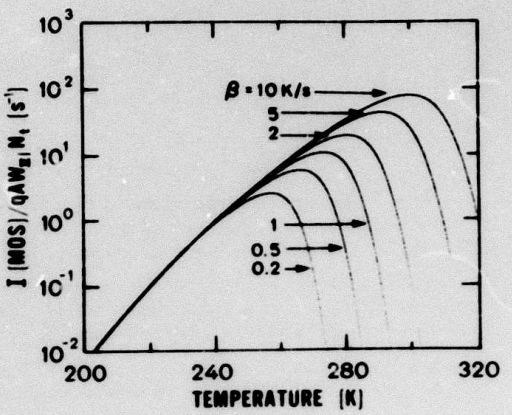



Figure 5. Calculated reduced phase II current from gold acceptor defects in an *n*-type silicon MOS capacitor as a function of temperature for $N_d/N_t$ = 100, H = 0.2, G = 1, and various values of β.

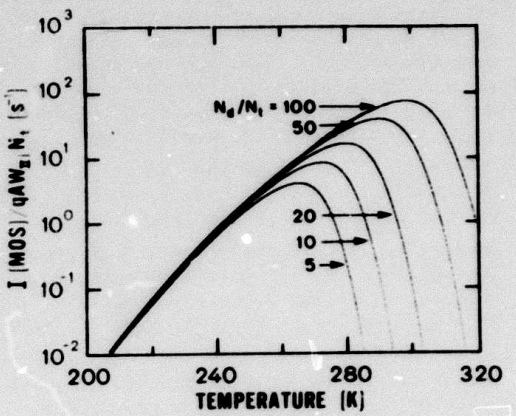



Figure 6. Calculated reduced phase II current from gold acceptor defects in an *n*-type silicon MOS capacitor as a function of temperature for β = 10 K/s, H = 0.2, G = 1, and various values of $N_d/N_t$.

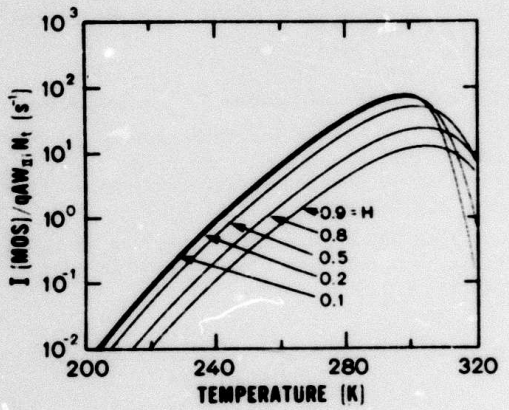



Figure 7. Calculated reduced phase II current from gold acceptor defects in an *n*-type silicon MOS capacitor as a function of temperature for β = 10 K/s, $N_d/N_t$ = 100, G = 1, and various values of H.

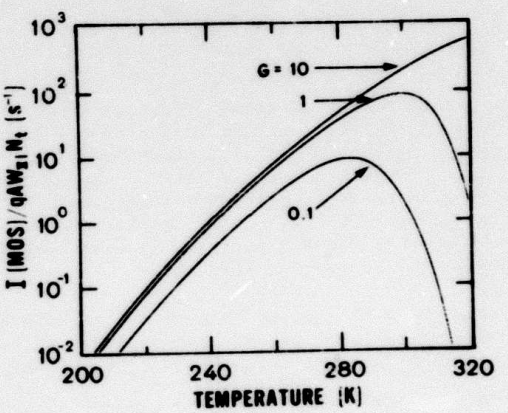



Figure 8. Calculated reduced phase II current from gold acceptor defects in an *n*-type silicon MOS capacitor as a function of temperature for β = 10 K/s, $N_d/N_t$ = 100, H = 0.2, and several values of G.

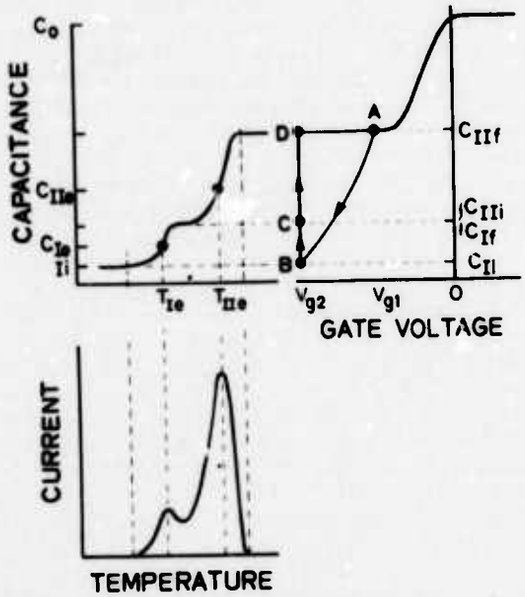



Figure 9. Capacitance-voltage characteristic and dynathermal current and capacitance response of an ideal gold-doped *n*-type silicon MOS capacitor.

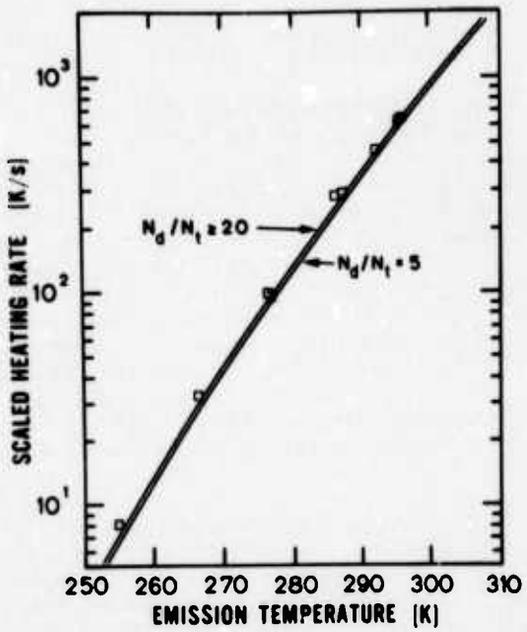



Figure 10. Scaled heating rate appropriate to obtain various emission temperatures during the phase II response from gold acceptor defects in an *n*-type silicon MOS capacitor. (Solid curves: theoretical; □: experimental, device 2107.7, $N_d/N_t$ = 25, F = 0.27, G = 0.90.)

Experimentally, the factor F was determined from the thermally stimulated current and capacitance response of a gold doped *n*-type MOS capacitor (Device 2107.7, NBS Spec. Publ. 400-1, p. 17). The results of the computations are presented in figure 10 in the form $\beta/F$ against $T_{IIe}$. Experimental data from device 2107.7 are also shown.

(W. E. Phillips and M. G. Buehler)

# 6. OXIDE FILM CHARACTERIZATION

## 6.1. X-Ray Photoelectron Spectroscopy

Considerable attention was given to determining the origin of the "carbide" carbon peak previously found on heated silicon specimens (NBS Spec. Publ. 400-4, p. 42). A sequence of carbon (1s), oxygen (1s) and silicon (2p) XPS scans on an air-stabilized silicon specimen were performed as a function of heating condition. Successive temperature levels were maintained for whatever period of time was necessary for outgassing to effectively cease. The heating was done in such a fashion that the total pressure in the chamber never exceeded $5 \times 10^{-7}$ Torr ($7 \times 10^{-5}$ Pa), starting from a base pressure of $3 \times 10^{-9}$ Torr ($4 \times 10^{-7}$ Pa).

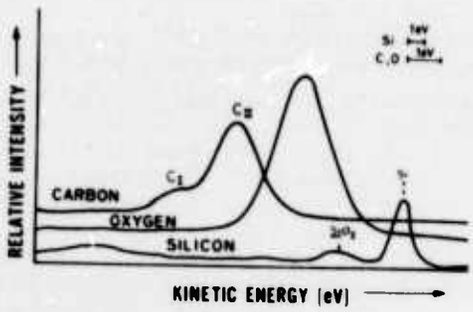
A quadrupole mass spectrometer was used to monitor the gas composition. During the initial heating, water was by far the major gas present; at higher temperatures, first hydrogen and then carbon monoxide became prominent. The evolution of carbon monoxide was accompanied by lesser amounts of hydrogen and water. After the specimen had been heated to approximately 1000°C, allowed to cool and then reheated, a short initial outgassing of hydrogen was observed, followed by an intense evolution of carbon monoxide. No evidence of an abundant hydrocarbon mass peak was observed at these higher temperatures. At temperatures below 400°C several unidentified mass peaks were present which could be due to outgassing from the silicon specimen, the molybdenum electrical contact spring in the specimen holder, or both.

Measurements of the silicon surface during heating indicated large amounts of carbon and oxygen with some silicon (di)oxide ($\underline{Si}O_2$), figure 11a. Mild heating to 870°C, figure 11b, caused the carbon peaks to decrease. The oxygen signal appeared to increase, presumably because the overburden of carbon containing material was removed. Heating the specimen to 930°C, figure 11c, caused a profound change in the spectra. Most of the oxygen was lost, the silicon (di)oxide peak practically disappeared, and the smaller remaining carbon peak shifted to higher kinetic energies. At 960°C, figure 11d, there appeared a further loss in oxygen, a further shift in the carbon peak to higher kinetic energies characteristic of "carbide" carbon ($\underline{Si}C$) and the appearance of a new shoulder on the Si(2p) peak at the position expected for silicon as silicon carbide ($\underline{Si}C$). The specimen was then allowed to cool overnight. Spectra taken the next day before heating, figure 11e, showed that a considerable amount of low kinetic energy carbon and some additional oxygen had been deposited. On heating to 960°C, figure 11f, most of the elemental carbon was lost, some seemingly converted to carbide as manifested by the growth of the "carbide" carbon ($\underline{Si}C$) and silicon ($\underline{Si}C$) peaks. The intensity of the oxygen peaks was also observed to diminish until at 1000°C oxygen could not be seen on the surface, figure 11g. Although there was no apparent change in the total amount of carbon present on the surface, both a narrowing of the carbide carbon peak and a further growth of the carbide silicon peak were experienced. In an additional experiment, the silicon specimen was bombarded with argon to sputter all carbon from the surface and then annealed at 950°C. After allowing the specimen to sit overnight in the vacuum, a contamination layer appeared which was similar to that which appeared after the specimen was cooled overnight after heating to 960°C (fig. 11e). When the specimen was reheated to 960°C silicon carbide was again produced (cf fig. 11f). The conclusion is that most, if not all, of the silicon carbide that forms results from the interaction of residual carbon containing gases in the spectrometer with the silicon surface.

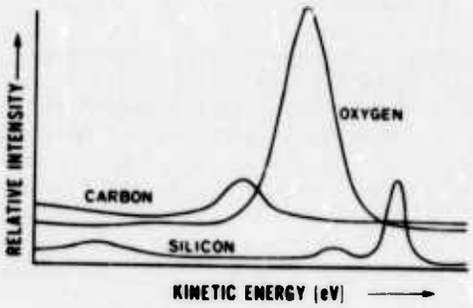
The large surface carbon to surface oxygen ratio observed before heating is too large to be due to a simple deposition of carbon monoxide, although carbon monoxide was the only carbon containing gas indicated by the mass spectrometer. One possibility is that the carbon monoxide dissociates on the silicon with a loss of oxygen from the surface. Another is that the hydrogen which evolved during the initial stages of reheating is not only the result of thermal desorption from the silicon and/or molybdenum surfaces but could be due to a cracking of some adsorbed hydrocarbons such as methane, ethane, ethylene, or even acetylene. Thus, although the exact gaseous species responsible for the formation of silicon carbide has not yet been identified, it does seem clear that the majority of the carbide comes not from the bulk of the silicon but instead is a reaction product with an as yet unidentified residual gas in the spectrometer.

(N. E. Erickson*, A. G. Lieberman, T. E. Madey*, and J. T. Yates, Jr.*)

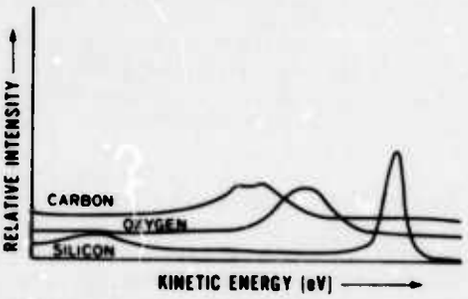
* NBS Surface Processes and Catalysis Section, Physical Chemistry Division.



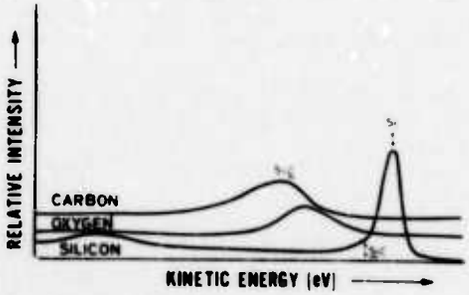

a. Unheated specimen.



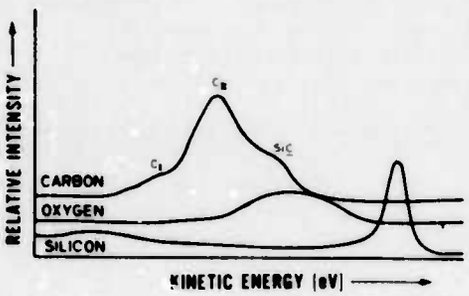

b. After heating to 870°C.



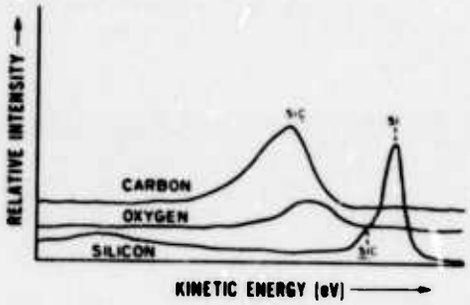

c. After heating to 930°C.



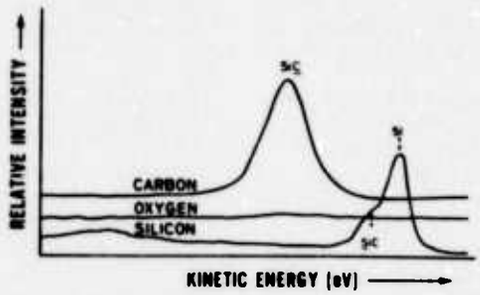

d. After heating to 960°C.




e. After cooling to room temperature in vacuum.




f. After reheating to 960°C.




g. After heating to 1000°C.

Figure 11. Metamorphoses of carbon 1s, oxygen 1s, and silicon 2p photoelectron peaks upon heating. (The energy scale covers 960 to 972.5 eV for the carbon spectrum, 710 to 722.5 eV for the oxygen spectrum, and 1130 to 1155 eV for the silicon spectrum.)

## 6.2. X-Ray Dose in Electron Beam Evaporators

Electron beam evaporation of aluminum in vacuum is widely used in the metallization process for fabricating semiconductor devices. Typically, the aluminum, held in a water cooled crucible, is melted by an electron beam with a beam energy and beam current of 10 keV and 0.5 A respectively. The electron bombardment, in addition to evaporating the aluminum, generates characteristic x-rays and bremsstrahlung radiation (a continuous spectrum of photons with energy $0 \leq E \leq$ electron beam energy) at the aluminum surface. The wafers being metallized are also exposed to some of this radiation.

The effect of the low energy radiation produced in the metallization process on the thermal oxides of MOS devices has been reported [15]. MOS transistor threshold voltage shifts of typically several volts were observed after aluminum evaporation. These shifts in threshold voltage were then removed by heating the metallized wafers to temperatures of 400°C or higher for short periods of time. However, a residual effect which affected the future radiation sensitivity of the device was observed in this experiment.

The purpose of the work reported here was to examine a measurement technique for determining the magnitude and characteristics of the radiation impinging on wafers during the metallization process by electron beam evaporation.

Using published data, an estimate of the energy deposited during metallization can be made. The yield, Y, of $K_\alpha$ x-rays emitted in the backward direction (laboratory angle $\theta_L$ = 180 deg or 120 deg) from aluminum bombarded by 10 keV electrons impinging normally to the surface (target angle $\alpha$ = 0 deg) is $2.4 \times 10^{-4}$ photons per steradian·electron [16]. These x-rays have an energy of 1487 eV ($2.382 \times 10^{-16}$ J). In an electron beam evaporator, the solid angle, $\Omega$, subtended by a 2 inch (5 cm) diameter wafer is approximately $10^{-2}$ sr; the exposure time may vary between 100 and 300 s depending on the evaporation rate and the thickness of metal film to be deposited. The energy $\Delta E$ (joules) deposited in a wafer by the aluminum $K_\alpha$ x-rays produced in this process (in joules) can be calculated from

$$\Delta E = YIt\Omega E(K_\alpha) \qquad (6)$$

where I is the beam current (amperes), t is the exposure time (seconds), and $E(K_\alpha)$ is expressed in electron volts. For an exposure time of 200 s and a beam current of 0.5 A, the energy deposited in the wafer is approximately 0.36 J. The energy deposited due to the continuous bremsstrahlung radiation is not included in this estimate since precise data are not available for 10 keV electrons interacting with thick aluminum targets; as will be shown later, the bremsstrahlung dose may be of approximately similar magnitude to that of the $K_\alpha$ radiation.

The energy deposited must be corrected for the shielding effect of the metal film on the wafer; as this film becomes thicker, it creates a protective shield against the radiation.

A preliminary experiment* to measure the radiation field present during the operation of an electron beam evaporator was performed using calcium fluoride thermoluminescent dosimeters (TLDs), 1/32 in. (0.79 mm) thick and 1/8 in. (3.2 mm) square. Ten TLDs were covered with Kapton† foils of varying thickness to avoid direct aluminization; for the purpose of this experiment the electron beam current was reduced to about 25 percent of the value normally used for metallization. These measurements yielded an absorption curve showing at least two components of the radiation field present during metallization in an electron beam evaporator; a short range component corresponding to 1.487 keV aluminum $K_\alpha$ characteristic radiation and a long range component corresponding to the continuous background. The evaporator parameters for this experiment are given in table 4 and the absorption curve is shown in figure 12.

---

* This experiment was performed with the assistance of Dr. M. Ehrlick, NBS Applied Radiation Division, who supplied the TLDs and the measuring equipment.

† This material is identified in this report in order to specify adequately the experimental procedure. Such identification does not imply recommendation or endorsement by the National Bureau of Standards, nor does it imply that the material is necessarily the best available for the purpose.

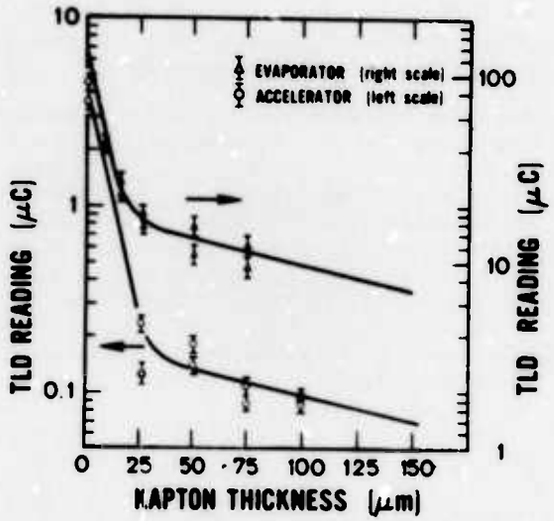



Figure 12. Absorption of x-rays generated by bombarding aluminum with 10-keV electrons.

Table 4 — Calibration of TLDs using the Backward Radiation from Thick Aluminum Target Bombarded by 10 keV Electrons

| | evaporator | accelerator |
|---|---|---|
| Beam energy, keV | 10 | 10 |
| Beam current, A | 0.15 | $2 \times 10^{-5}$ |
| Exposure time, s | 60 | 500 |
| $\theta_L$, deg | 120 | 180 |
| $\alpha$, deg | 0 | 0 |
| $\Omega$, sr | $4.8 \times 10^{-5}$ | $7.9 \times 10^{-5}$ |
| TLD reading, μC | 135 | 4 |

To convert the TLD readings to absorbed energy requires a calibration factor. The TLDs were calibrated[x] using the radiation emitted at 180 deg when 10 keV electrons from the NBS constant potential accelerator impinged normally ($\alpha$ = 0 deg) on a thick aluminum target. Using various thicknesses of Kapton as an absorber, an absorption curve similar to that resulting in the evaporator was measured. The results are also shown in figure 12. The zero-thickness reading was approximately 4 μC. From eq (6) with $Y = 2.4 \times 10^{-4}$ photons per steradian·electron, the total energy deposited is 2.8 μJ. The calibration constant for the TLDs is therefore 0.07 μJ/μC. The total energy deposited in the TLD in the evaporator corresponding to an extrapolated zero-Kapton-thickness reading of 135 μC is 9.5 μJ. If this is converted to the normal metallization conditions for a 2 in. (5 cm) wafer, the energy deposited on the wafer would be 0.02 J. Since this value does not compare favorably with the previously calculated value of 0.36 J, the discrepancy must be investigated. However, either of the values leads to a large radiation dose if the energy is uniformly incident on a film of silicon dioxide 100 nm thick on a 2 in. (5 cm) diameter silicon wafer. From cross-section data [17] the fraction of incident energy absorbed in the oxide can be calculated to be 2.4 percent. Therefore, the absorbed dose in the oxide is about $1.8 \times 10^4$ J/kg ($1.8 \times 10^6$ rads($SiO_2$)) for incident energy of 0.36 J and about $10^3$ J/kg ($10^5$ rads($SiO_2$)) for incident energy of 0.02 J. This estimate does not include the bremsstrahlung contribution.

The shielding effect of the deposited aluminum is rather small for the aluminum $K_\alpha$ radiation since a 1 μm thick aluminum film transmits about 96 percent of the incident 1.5 keV photons. The low energy portion of the bremsstrahlung continuum, however may be absorbed by the deposited aluminum. Since the photon distribution with energy in the bremsstrahlung continuum is not known, it is difficult to assess the dose absorbed in the oxide. However, it seems likely from the data obtained in this preliminary experiment that an additional dose of approximately similar magnitude to that of the $K_\alpha$ radiation arises from the bremsstrahlung continuum.

(S. Mayo)

[x] The calibration was performed in collaboration with Dr. C. E. Dick, NBS Applied Radiation Division.

# 7. TEST PATTERNS

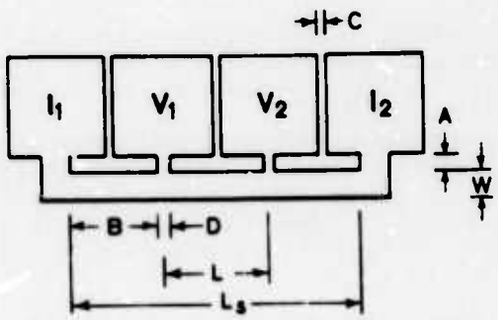
## 7.1. Sheet Resistors

As part of a study of the structures on test pattern NBS-3 (NBS Spec. Publ. 400-12, pp. 19-22), an analysis was undertaken of the four base sheet resistors (devices 3.11, 3.22, 3.28, and 3.30). The analysis included an intercomparison of sheet resistance values which showed that van der Pauw structures [18] whose active areas differ by forty times yield values that generally differ by less than 1 percent. In addition, the width of the base diffusion window as determined by electrical measurements on van der Pauw and bridge structures was found to agree with measurements made on photomicrographs. The electrical measurements are sensitive to width changes that are smaller than 5 μin. (0.12 μm). These measurements are important in the manufacture of semiconductors because of the significance of control of dimensions in designing and fabricating devices.

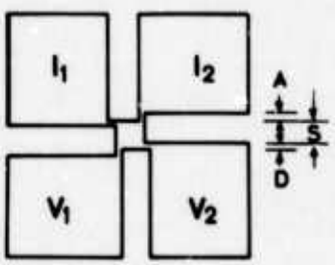
Base sheet resistors were fabricated in nominally 5 Ω·cm, n-type (111) silicon substrates on which a 300 nm thick oxide was grown in steam at 1100°C. Base diffusion windows were etched in the oxide using a buffered hydrofluoric acid solution for 3 min. The boron nitride, predeposition base diffusion was at 965°C for 25 min in dry nitrogen. After a deglaze in 10 percent hydrofluoric acid solution, the base drive-in diffusion was at 1100°C for 18 min in wet oxygen, followed by 40 min in dry oxygen, followed by 15 min in dry nitrogen. After a subsequent phosphorus emitter diffusion at 1000°C for 20 min and a reoxidation at 925°C for 45 min. followed by contact window opening and aluminum metallization, the base sheet resistance was about 175 Ω/□ and the junction depth as measured by the angle lap and stain method [19] was about 2.1 μm.

Line drawings of sheet resistors 3.22 and 3.28 are shown in figure 13. The bridge structure (3.28) was designed where possible in accordance with the ASTM standard [20] which requires that $W \geq 3D$, $L_S \geq 5W$, and $B \geq 2W$. In addition, the following are required to minimize lateral diffusion and over-etch effects: $L \geq 10X_j$, $A \geq 5X_j$, and $C \geq 5X_j$, where $X_j$ is the junction depth. Analysis of the potential distribution in the van der Pauw structure (3.22) by means of a conducting paper analog indicated that it is necessary to have $S \geq 3D$ and $A \geq S/2$ to insure that the error in the calculated resistivity is less than 1 percent. Both sheet resistors 3.22 and 3.28 have rectilinear boundaries to facilitate reproduction by computerized pattern generation.

The sheet resistance was measured by the dc four-probe method. Current was passed between contacts $I_1$ and $I_2$, shown in figure 13, and the potential between contacts $V_1$ and $V_2$ was measured by means of a digital voltmeter with 1 μV resolution. The linearity of the current-voltage characteristics was studied for various values of current. It was established that a current of 100 μA is within the linear range of these resistors and produces a stable, noise-free voltage reading greater than 1 mV. In the case of van der Pauw structures, an additional measurement must be made with the contact positions rotated 90 deg. In every configuration, the current is reversed to confirm the linearity of the current-voltage relationship. Measurements were made on the same wafer as quickly as possible so as to minimize room temperature drift effects. For resistors 3.22 and 3.28 measurements




a. Bridge structure (3.28). The center-to-center pad spacing is 6 mil (0.15 mm).




b. Orthogonal van der Pauw structure (3.22). The center-to-center pad spacing is 8 mil (0.20 mm).

Figure 13. Scaled line drawings of base sheet resistor structures or test pattern NBS-3 showing critical dimensions.

were made in room light and with grounded substrates. For resistors 3.11 and 3.30, measurements were made in the dark using ungrounded substrates. These conditions are necessary when significant junction leakage exists as in resistor 3.30 which has a junction area significantly larger than that of resistor 3.28. The field plate of resistor 3.11 was shown to have negligible influence on the measured sheet resistance; it was permitted to float during the measurements.

For the van der Pauw structure, the sheet resistance was computed from [18]

$$R_S(VDP) = \frac{\pi}{\ln 2} \left.\frac{V}{I}\right|_{VDP}, \qquad (7)$$

where the voltage current ratio is averaged for both directions of current and for both contact orientations. For the bridge structure the sheet resistance is computed from

$$R_S(B) = \frac{W + \alpha X_j}{L} \left.\frac{V}{I}\right|_B, \qquad (8)$$

where L can be taken equal to the mask dimension L(mask) because it is not affected by lateral diffusion or over etching. However although the width W is greater than the mask dimension:

$$W = W(mask) + \alpha X_j + W_{oe}, \qquad (9)$$

where $W_{oe}$ accounts for over etching and $\alpha X_j$ (with $\alpha = 0.3$ and $X_j$ the junction depth) accounts for lateral diffusion [21], W is frequently taken as W(mask).

Sheet resistance values as a function of position across a wafer are shown in figure 14. The sheet resistance values for the bridge structure were calculated from eq (8) using the nominal mask dimensions, W = W(mask) = 1.5 mil (38 μm) and L = L(mask) = 6.0 mil (152 μm). The general shape of all the curves is the same, but the sheet resistances measured on the three van der Pauw structures are tightly clustered while the value measured on the bridge structure is significantly lower. This result suggests that the true value of W is significantly greater than W(mask).

In order to test the sensitivity of these resistors to over etching of the base diffusion window, etch times were chosen so that one wafer was etched for 3 min, another wafer for 6 min, and a third wafer for 9 min. The sheet resistance values shown in figure 15, were computed as before using the mask dimensions for W and L in computing sheet resistance from measurements on the bridge structure. The results show that the

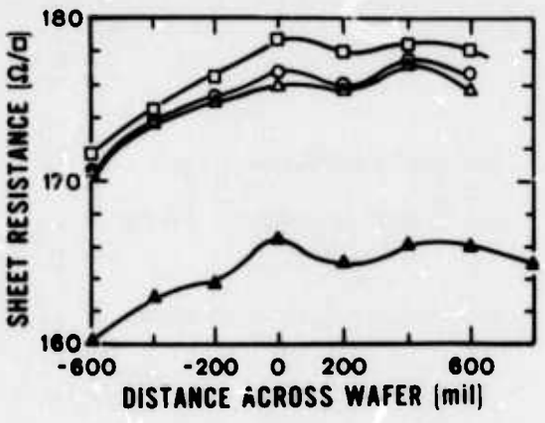



Figure 14. Sheet resistance as a function of position along a wafer diameter. (van der Pauw structures: □, 3.30; ○, 3.22; △, 3.11; Bridge structure: ▲, 3.28.)

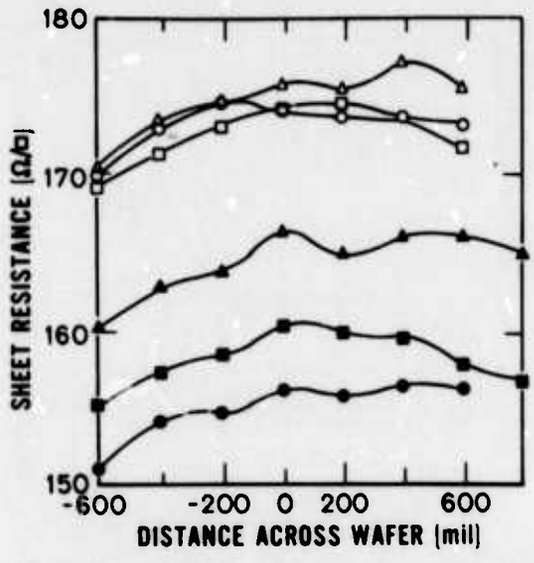



Figure 15. Sheet resistance as a function of position along the diameter of wafers etched for different times. (△, □, ○: van der Pauw structure (3.22); ▲, ■, ●: Bridge structure (3.28); △, ▲: 3-min etch; □, ■: 6-min etch; ○, ●: 9-min etch.)

measurements on the bridge structure (3.28) are sensitive to the time used to etch the base diffusion windows while the measurements on the van der Pauw structure (3.22) are not.

Equating $R_s$(B) and $R_s$(VDP) and combining eqs (7)-(9), with L = L(mask) leads to

$$W = L(\text{mask})\ R_s(\text{VDP})\ \frac{I}{V}\bigg|_B - \alpha X_j. \qquad (10)$$

Figure 16, demonstrates the effect of increased etch time on the width of the base diffusion window as determined from measurement of $R_s$(B) and $R_s$(VDP). The measurements were repeatable to within the range covered by the open circles on the figure.

As an independent check of the diffusion window widths calculated from the electrical measurements, measurements were made directly on photomicrographs of various test structures. An optical microscope with a 40X objective was operated in the Nomarski differential interference contrast mode. The magnification as measured on the photomicrograph was 585X. From these photomicrographs it was established that test structure dimensions determined from "like boundaries" are transferred from photomask to wafer with a tolerance better than ±20 μin (±0.5 μm). Pairs of like boundaries, labeled A and C and D and E in figure 17, are such that the degree of etching does not affect the distance between such boundaries. The distance L in eq (10) is a distance between like boundaries and therefore can be taken directly from the photomask dimensions.

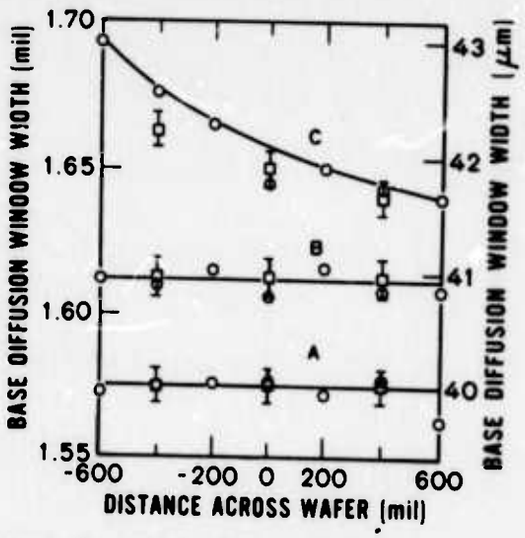



Figure 16: Width of base diffusion window as measured electrically using eq (10) with $X_j$ = 0.083 mil (2.1 μm) (O) and from photomicrographs (□) along the diameter of wafers etched for different times. (A: 3-min etch; B: 6-min etch; C: 9-min etch.)

The boundaries between oxide levels had a finite width as shown in figure 17. Since it was assumed that the edges of the base diffusion window occurred at the centers of the appropriate transition regions, the distance between edges B and C corresponds to the width of the base diffusion window. In measuring this width, the distance between edges A and C was taken from the photomask dimensions. A scale was placed on the photomicrograph at an angle such that the distance between A and C was a convenient multiple of the actual dimension. The distance between C and B could then be read directly from the scale. The values obtained are plotted as open squares in figure 16. The error bars shown correspond to one-fourth the distance between scale divisions. Both sets of values are in good agreement and are larger in all cases than W(mask). These results illustrate that the electrical width measurements are sensitive to width changes smaller than 5 μin. (0.12 μm). In addition they can be made quickly and at low cost using available automatic equipment. Thus, these measurements are important in the manufacture of semiconductors because of their potential use as process control and device design vehicles. (M. G. Buehler)

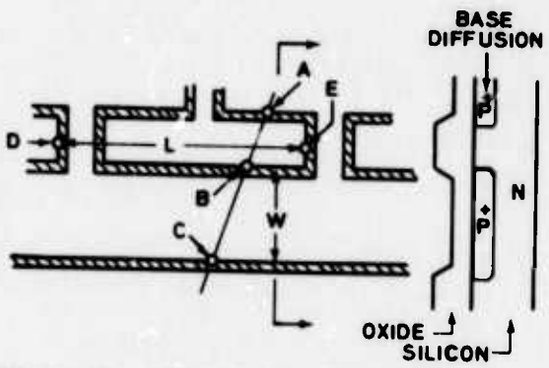



Figure 17. Expanded schematic views of the bridge sheet resistor structure illustrating the measurement of L and W from the photomicrographs. (The boundaries, shown cross-hatched, are exaggerated in width for clarity.)

## 7.2. Square Array Collector Resistor

Structure 3.17 of test pattern NBS-3 (NBS Spec. Publ. 400-12, pp. 19-22) is a square four-probe array designed to measure the resistivity of the undiffused or collector region of the pattern. The probes are narrow pipes of undiffused material surrounded by a base diffusion of opposite type as shown in figure 18. Emitter areas are diffused into each pipe to give a low resistance contact to the collector material.

The measurement consists of passing current between two adjacent probes, $I_1$ and $I_2$, and measuring the voltage between the other two probes, $V_1$ and $V_2$. Assuming the substrate to be semi-infinite in extent, the resistivity $\rho$ is determined from [22]

$$\rho = \frac{2\pi s}{2 - \sqrt{2}} \frac{V}{I} = 10.726\ s \frac{V}{I},$$

where s is the probe spacing, V is the measured voltage, and I is the current. The voltage is measured for both directions of current and averaged. Also for accurate results it is necessary to rotate the electrical connections ninety degrees and average the two sets.

The pipe regions are protected from the 1 to 2 μm deep base diffusion by squares in the base mask which are 0.25 mil (6.3 μm) on a side. However, the pipe dimensions are reduced by lateral diffusion of the base, and the effective cross sectional area of the pipe is further reduced by the depletion region associated with the base-collector junction. This causes a large voltage drop along the pipe even at low currents. Above some current (which depends on resistivity since both the lateral diffusion and the depletion width increase with increasing collector resistivity but can be quite low because of the large voltage drop) the emitter-base junction breaks down, the measured voltage saturates, and the calculated resistivity is below the actual value. For each wafer, a current large enough to provide a measurable voltage but small enough to avoid breakdown is chosen on the basis of preliminary measurements.

The probe spacing used in the calculations is the center-to-center distance of 2.250 mil (57.15 μm) between the collector pipes as taken from the design dimensions. The four probe spacings were checked by measurements on a photomicrograph of the base mask and found equal to the design value within about

a. Photomicrograph. (Magnification: ~135X.)

b. Photomicrograph of pipe region. (Magnification: ~675X.)


c. Schematic cross section, scaled in horizontal direction only.

Figure 18. Square array collector resistor structure.

Table 5 - Comparison of Resistivity Measured by Square Array Test Structure with Resistivity Measured by Four-Probe Method Before Processing

| Slice No. | Four-Probe[a] | Square Array | % diff[b] |
|---|---|---|---|
| A0.27Ph-1 | 0.287±0.010 | 0.276±0.019 | -3.83 |
| A1.0Ph-1 | 1.013±0.012 | 1.007±0.030 | -0.59 |
| 5200 | 5.34±0.08 | 5.19±0.12 | -2.81 |

[a]Before processing.

[b][(Square Array)/(Four-Probe) - 1] × 100.

0.5 percent. Based on calculations by Uhlir [22], the error due to finite wafer thickness is less than one percent for the wafers used which are typically about 10 mil (0.25 mm) thick and have a conducting back side.

Measurements were made on three $n$-type wafers being used for the reevaluation of the resistivity-dopant density relationship (sec. 4.4.). Before processing, the resistivity of each wafer was measured along two perpendicular diameters by the four-probe method [7] corrected for off-center position [23]. After the test pattern was fabricated, resistivity measurements were made on two or more square-array structures located near the center of the wafer. The results are summarized in table 5. The variability indicated for the four-probe measurements is the sample standard deviation of the values at the center of the wafer and at four points 200 mils (5.1 mm) from the center in each direction. The variability indicated for the square-array measurements is the sample standard deviation of measurements made on the structure located nearest to the center of the wafer and three, four, or one adjacent devices located on perpendicular diameters for wafers A0.27Ph-1, A1.0Ph-1, or 5200, respectively. Previous experience with material in this resistivity range has shown that processing does not significantly change the resistivity.

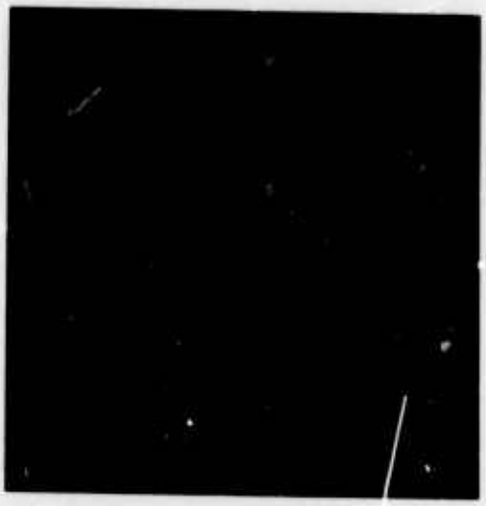
(W. R. Thurber, Y. M. Liu, and M. G. Buehler)

## 7.3. MOS Capacitor Over Collector

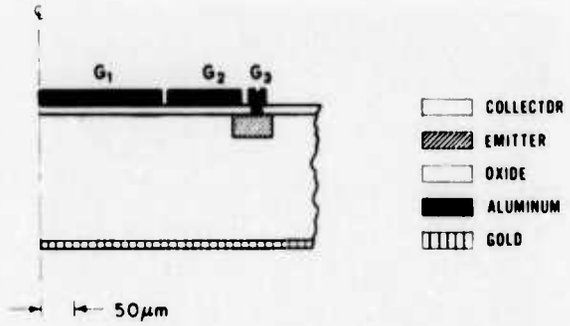
Structure 3.8 of test pattern NBS-3 (NBS Spec. Publ. 400-12, pp. 19-22) is an MOS capacitor over the undiffused or collector region of the wafer. This structure can be used to measure the dopant density in the wafer. The structure, illustrated in figure 19, consists of a central gate electrode, $G_1$, 15.0 mil (381 μm) in diameter over a uniform layer of oxide which is typically 0.3 to 0.5 μm thick. A circular emitter diffusion outside the gate electrode provides a heavily doped region of the same conductivity type as the collector which serves together with a metal ring, $G_3$, as the topside collector contact. Between $G_1$ and $G_3$ there is a circular field plate, $G_2$, 4.5 mil (114 μm) wide, which is separated from $G_1$ by 0.5 mil (13 μm) and extends over the edge of the emitter ring. A backside collector contact is also provided.

Typical use of this structure consists of measuring the capacitance, C, as a function of the applied bias voltage, V, on $G_1$, which is scanned uniformly from accumulation to inversion and back. When using a three terminal capacitance bridge, the gate $G_1$ is the "HI" electrode and either $G_3$ or the backside contact is the "LO" electrode; if the backside contact is used, $G_3$ is left floating, and vice-versa. The field plate, $G_2$, is biased according to the needs of the situation. For an $n$-type MOS capacitor, $G_2$ is usually grounded since the surface is accumulated at zero bias. For a $p$-type MOS capacitor it is necessary to bias $G_2$ with sufficient negative voltage to cause accumulation at the surface. This is illustrated in figure 20 which shows C-V characteristics for a $p$-type MOS capacitor under different bias conditions on $G_2$.

At a bias on $G_2$ more negative than the flat-band voltage, $V_{fb}$ (-18 V in this case), the true high frequency C-V characteristic is obtained as illustrated by the curve labeled $V_{G2} = -20$ V in the figure. From this curve, it is possible to derive the dopant density within a depletion depth of the surface of the collector region by means of the usual



a. Photomicrograph. (Magnification: ~90X.)




b. Schematic cross section, scaled in horizontal direction only.

Figure 19. MOS capacitor over collector structure.

$C_{max} - C_{min}$ method (NBS Spec. Publ. 400-4, pp. 37-38).

If the rate of scanning $V_{G1}$ is increased so that it is high enough to prevent minority carrier equilibrium, the deep depletion characteristic ($C_D$ in fig. 20) is obtained. From this curve, the dopant density characteristic of the bulk of the undiffused collector region can be determined by means of the dynamic MOS C-V method (sec. 4.2.).

(R. Y. Koyama and M. G. Buehler)

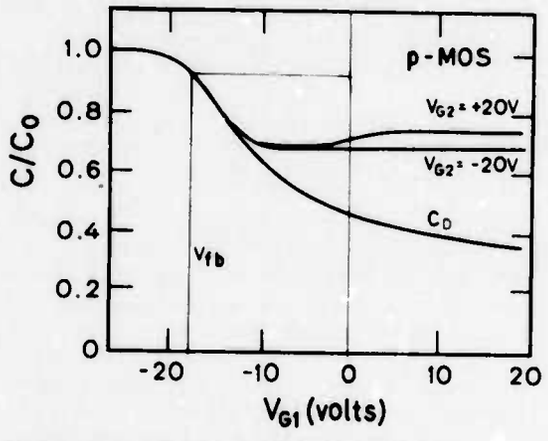


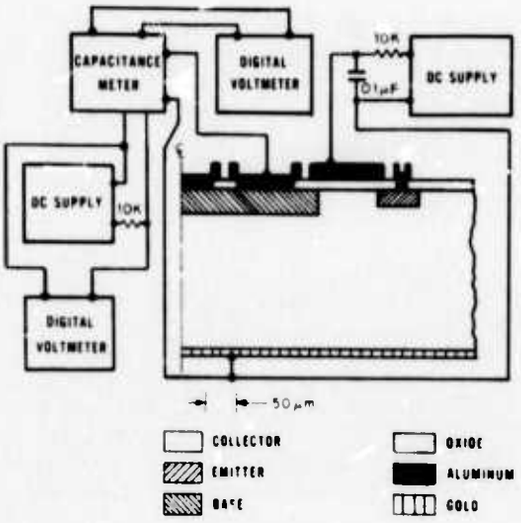

Figure 20. Typical high-frequency capacitance-voltage characteristics of a $p$-type silicon MOS capacitor showing the effect of surface inversion around the periphery ($V_{G2}$ = +20 V), the true equilibrium characteristic ($V_{G2}$ = -20 V), and a non-equilibrium, deep depletion characteristic ($C_D$). ($C_o$ = 12.4 pF, $V_{fb}$ = -18 V.)

## 7.4. Base-Collector Diode

Structure 3.10 of test pattern NBS-3 (NBS Spec. Publ. 400-12, pp. 19-22) is a base-collector diode from which the dopant density in the undiffused or collector region of the pattern can be measured by the junction C-V method. The structure, which is illustrated in figure 21, consists of a 17.0 mil (432 μm) diameter diffused base region of conductivity type opposite to that of the collector to form a $p^+n$ or $n^+p$ junction. The junction depth is typically 2 μm. Contact to the diffused region is made by means of an aluminum ring and disc configuration evaporated into windows cut in the oxide. Contact to the collector region is made either by means of a doped gold layer alloyed to the backside of the wafer or an emitter ring diffusion on the topside of the wafer. The emitter ring, which is of the same conductivity type as the collector, also serves to limit the formation of surface channels outside the active region of the structure. Between the base diffusion and the emitter ring there is a circular aluminum electrode (gate) over the oxide to control the surface near the junction (NBS Tech. Note 788, pp. 9-11).

When capacitance-voltage (C-V) measurements are being made, the device is connected in the manner shown in figure 21b. The gate is held at ac ground and biased by a low impedance voltage supply at some suitable voltage such as the flat band voltage. The 10 kΩ series resistor serves to limit the current in event the gate is shorted to the collector. Bias is applied to the $p$-$n$ junc-

a. Photomicrograph. (Magnification: ~90X.)




b. Schematic cross section, scaled in horizontal direction only, and block diagram of measurement circuit.

Figure 21. Base-collector diode.

tion through the capacitance meter. The 10 kΩ series resistor serves to limit the junction current when breakdown occurs. The capacitance is read using a digital voltmeter connected to the analog output of the meter. A second digital voltmeter is used to read the junction bias voltage. A dopant density profile is then calculated from the C-V data using a BASIC computer program which includes appropriate corrections for peripheral effects and for back depletion into the diffused layer [24].

(R. L. Mattis and M. G. Buehler)

## 7.5. Charge-Coupled Device Test Pattern

This study was undertaken to investigate the applicability of the charge-coupled device (CCD) as a test structure for use in semiconductor process control. Before the CCD is considered for use as a process control tool, the parameters measured from the CCD must be correlated with those measured by other, better known, devices such as MOS capacitors and MOS transistors. During this quarter a model was developed for the CCD operating as an MOS capacitor and comparisons of characteristics derived from measurements on a CCD were made with characteristics derived from measurements on MOS capacitors and MOS transistors fabricated on the same wafer (NBS Spec. Publ. 400-8, pp. 26-27).

When the CCD is operated as a capacitor, the capacitance is measured between the phase three electrodes, connected to the aluminum interconnect, and the substrate. The equivalent circuit model for this configuration consists of the following five capacitors connected in parallel:

1. Thin oxide/$p^-$ substrate
2. Thick oxide/$p^-$ substrate
3. Thin oxide/$p^+$ channel stop diffusion
4. Thick oxide/$p^+$ channel stop diffusion
5. Thick oxide/$n^+$ interconnect diffusion

These capacitors can be identified in the cross sectional view through a phase three electrode shown in figure 22.

The MOS capacitors formed over the $p^-$ substrates are voltage sensitive, but those formed over the $p^+$ and $n^+$ diffusions are assumed to be insensitive to voltage and have capacitance values taken as the oxide capacitance. It should be noted that the MOS capacitor formed over $p^-$ substrates includes the capacitance contributed by the bonding pad. Because the $n^+$ phase one and phase two interconnect diffusions are grounded (NBS Spec. Publ. 400-12, pp. 22-23), the capacitance associated with these capacitors is eliminated from the measurement.

The CCD can also be operated as a capacitor by using the input gate electrode. In this

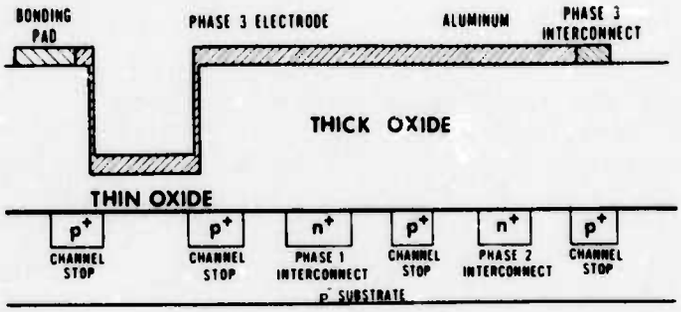



Figure 22. Cross sectional view through phase 3 electrode of CCD test structure.

configuration, the model must include the first four capacitors listed above, but the areas of each are different.

The analysis of the MOS capacitance-voltage characteristics of the CCD (NBS Spec. Publ. 400-12, pp. 23-24) using the above equivalent circuit model involves evaluating the area of the metallization over each region, the thickness of the thin and thick oxides, and the $p^-$ substrate dopant density. The area of the metallization over each region was determined from the artwork supplied to the photomask manufacturer; the procedure ignores lateral diffusion and over-etch effects (sec. 7.1.). The area calculated for each of the capacitors identified above is given in table 6 along with the areas of the two MOS capacitors which were used in the subsequent correlation studies.

The two oxide thicknesses were determined from two capacitance measurements on the CCD in the accumulation region, one using the phase three electrodes and the second using the input gate. These measurements provide capacitance values for two equations containing the two unknown oxide thicknesses. To determine the $p^-$ substrate density the CCD was connected as an MOS capacitor biased into inversion. Care was taken to apply enough bias so that both thin and thick MOS capacitors were inverted. To obtain the thin oxide inversion capacitance, the three other capacitances described above were subtracted from the measured inversion capacitance using the appropriate areas and oxide thicknesses. The substrate dopant density was determined using the thin oxide capacitance, the thin oxide inversion capacitance, and the strong inversion approximation (which states that the onset of inversion occurs when the surface potential is twice the difference between the bulk and intrinsic Fermi potentials.)

The results of these measurements on one 32-bit circular CCD (device 2) on wafer 1 are summarized in table 7. For comparison, average values of dopant density and oxide thickness obtained from measurements on about 15 thin oxide MOS capacitors (device

Table 6 - Metallization Area

| Device<br>Device Number | MOSCAP<br>21 | MOSCAP<br>13 | CCD (PHASE 3)<br>2 | CCD (INPUT GATE)<br>2 |
|---|---|---|---|---|
| Thin Oxide $p^-$ | — | $6.59 \times 10^{-4}$ cm$^2$ | $7.39 \times 10^{-5}$ cm$^2$ | $2.42 \times 10^{-6}$ cm$^2$ |
| Thick Oxide $p^-$ | $2.06 \times 10^{-3}$ cm$^2$ | — | $2.90 \times 10^{-4}$ | $2.09 \times 10^{-4}$ |
| Thin Oxide $p^+$ | — | — | $2.44 \times 10^{-5}$ | — |
| Thick Oxide $p^+$ | — | — | $1.65 \times 10^{-4}$ | $1.28 \times 10^{-6}$ |
| Thick Oxide $n^+$ | — | — | $6.33 \times 10^{-5}$ | — |

Table 7 - MOS Capacitor Parameters (Wafer 1)

| Device<br>Device Number | CCD[a]<br>2 | MOSCAP[b]<br>21 | MOSCAP[b]<br>13 |
|---|---|---|---|
| Substrate Dopant Density, $cm^{-3}$ | $1.6 \times 10^{16}$ | $(9.4 \pm 0.6) \times 10^{15}$ | $(8.5 \pm 0.4) \times 10^{15}$ |
| Thin Oxide Thickness, Å | 1200 | — | 950±30 |
| Thick Oxide Thickness, Å | — | 7770±20 | — |

[a]Single measurement.

[b]Mean value ± one sample standard deviation of measurements on about 15 capacitors of each type.

Table 8 - MOS Transistor Parameters (Wafer 3)

| Device<br>Device Number | MOSFET<br>26 | CCD<br>2 |
|---|---|---|
| Operation: Linear Region | | |
| $V_T$, V | 0.26 | 0.19 |
| $X_o$, A (Thin Oxide) | 950[a] | 960[b] |
| W/L | 31.4[c] | 0.044 |
| $\mu_n$, $cm^2/V \cdot s$ | 590 | 590 |
| Operation: Saturation Region | | |
| $V_T$, V | 0.11 | 1.1 |
| $X_o$, A (Thin Oxide) | 950[a] | 960[b] |
| W/L | 31.4[c] | 0.044 |
| $\mu_n$, $cm^2/V \cdot s$ | 660 | 440 |

[a]Determined from measurements on device 13 on Wafer 1.

[b]An average value where depletion in the $p^-$ region under the thick oxide was not included.

[c]Calculated from the photomask dimensions, W(mask) = 10.0 mil (254 μm) and L(mask) = 0.400 mil (10.16 μm), corrected to account for lateral diffusion; end effects were ignored.

13) and thick oxide MOS capacitors (device 21) on wafer 1 are also listed in the table.

Threshold voltages and channel mobilities were determined from measurements on a 32-bit circular CCD (device 2) (on wafer 3) operated as an MOS transistor and correlated with similar quantities determined from measurements on an MOS field effect transistor (device 26) on the same wafer. The operation of the 32-bit circular CCD as an MOS transistor consists of holding all electrodes and the output gate at a dc potential (45 to 50 V) and stepping the input gate (1 to 10 V). Oscilloscope traces were obtained by this method and parameters determined in the linear and saturation regions using the mathematical relations presented previously (NBS Spec. Publ. 400-12, pp. 23, 25).

The results of this analysis are shown in table 8 where the arrows indicate how results were combined to obtain the channel mobilities. For the MOS transistor, the channel mobilities in both the linear and saturation regions were calculated from the appropriate equations; the oxide thickness was assumed as the value found from measurements on the MOS capacitor (device 13) on wafer 1, and the W/L ratio was calculated from the photomask dimensions with L reduced by 2 μm and W increased by 2 μm to allow for lateral diffusion (end effects were ignored).

The W/L ratio for the CCD was obtained using the channel mobility of the MOS transistor operating in the linear region and the oxide thickness determined from measurements on the CCD connected as an MOS capacitor. This ratio was found to be close to the design value of about 0.01. This value of W/L and the same value of oxide thickness were used to calculate the channel mobility for the drain current in the saturation region.

(I. Lagnado* and M. G. Buehler)

---

* Naval Electronics Laboratory Center, San Diego, California. Work conducted under NBS Order No. 502498.

# 8. PHOTOLITHOGRAPHY

## 8.1. Automated Photomask Inspection

Detailed analyses were begun of the state-of-the-art technologies previously identified (NBS Spec. Publ. 400-4, pp. 49-50) as applicable to automated photomask inspection. The objects of these analyses are to assess the soundness of the physicsl principles on which a specific technology is based, to identify the limitations of each technology in the ability to detect photomask defects and the time required to do this, and to identify areas where improvements could be made.

The smallest visual defect dimension to be detected was chosen to be 2 μm. This dimension wss chosen since defects of this size or larger may be expected to print on a wsfer while smaller defects generally will not print [25]. The precision of registration of successive photomask functional patterns was chosen to be ±0.25 μm or less which is the registration criterion that is now widely used in the industry [26]. Both surface imperfections and surface flatness were considered in assessing the applicability of a technology to photoplate inspection.

The first technology analyzed consisted of a system which employs a TV camera tube to view the array of patterns through a microscope. The photomask is on a movable stage which is stepped across the field of view of the microscope. The photomask pattern information is imaged on the tube target, digitized, and compared with data representing the correct pattern that is stored in a computer memory. This technology has its primary application in visual defect detection. It may be applied to registration inspection if the position of the stage is known to sufficient accuracy which involves the use of either a linear encoder or a laser interferometrically controlled stage. A schematic diagram of this system is shown in figure 23.

The required resolution of the microscope objective is determined by the smallest dimension, $\delta$, of the defect that is to be detected. This resolution determines the minimum value of the numerical aperture, $NA_{min}$, of the objective:

$$NA_{min} = 1.2\lambda/\delta ,$$

where $\lambda$ is the wavelength of the light used to view the image. This equation is based on the criterion that the light intensity be zero between the nearest two points to be resolved [27]. For a 2 μm defect criterion and $\lambda$ = 0.55 μm, a numerical aperture of 0.33 or larger is required.

The magnification of the microscope objective, $M_{obj}$, may be selected from a host of commercially available objectives provided the numerical aperture criterion is satisfied. Another critical factor is the field of view of the objective because it is this that determines in part how fast the mask may be inspected. An objective with a higher magnification produces a larger image at

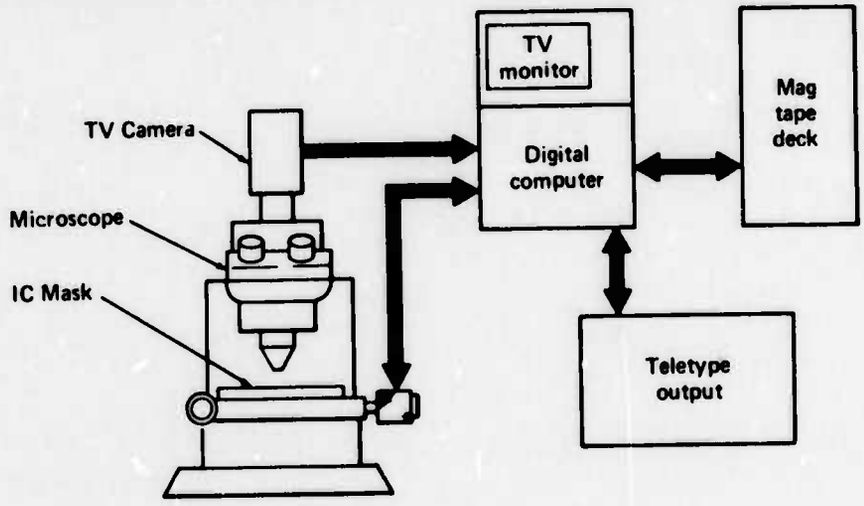



Figure 23. Block diagram of TV/microscope automatic mask inspection system.

the expense of reducing the size of the field of view.

An image of the patterned mask is projected onto the tube target through the microscope. To utilize the tube efficiently the projected image must fill the target area which is usually square or rectangular. Consequently, the smaller target dimension, t; the side, s, of the square inscribed in the circular field of view of the microscope objective; and the total optical magnification of the microscope, $M_{tot}$, are related by

$$M_{tot} = t/s \ .$$

The smallest image dimension that must be resolved by the tube, $R_r$, is the product of the smallest defect dimension, $\delta$, times the total optical magnification:

$$R_r = \delta M_{tot} \ .$$

The minimum number of scanned lines per millimeter, $\ell$, is the reciprocal of this product. Calculated values for comparison of these parameters are given in table 9 for 20 by 20 mm target and selected values of $\delta$ and $M_{obj}$. For these calculations $\lambda$ was chosen as 0.55 μm, and the values of s were calculated assuming fields of view of typical microscope objectives [27].

The resolution of the TV tube and its modes of operation are dependent on the tube design and construction. Both vidicon and image dissector tubes are compatible with this technology and each offers different advantages.

The target of the vidicon tube is coated with a photoconductive coating such as antimony trisulfide or lead oxide. This target is given a uniform negative charge by sweeping an electron beam across it; when a light image is projected on the target, the target coating discharge is proportional to the light intensity. This charge pattern is retained on the target; a sweeping electron beam recharges the screen. The beam current necessary to recharge an area of the screen and the coordinates of the recharged area provide data that are digitized and read into a computer. In this image data gathering process the charge pattern is erased. Before data on a new target image can be taken, it is necessary for the target to be uniformly charged. Consequently, the entire target area must be swept a second time by the electron beam before a new image is projected on it. The tube cycle time is the sum of the time necessary to read the charge pattern information and the time necessary to completely erase the previous image. One property of the vidicon is that the target charge pattern remains after the target illumination ceases. Thus, stroboscopic techniques may be used with this tube.

The image dissector tube target is coated with a photocathode material, generally some combination of sodium, potassium, cesium, and antimony. When a spot of light strikes the target, electrons are released and are focused onto an anode plate containing an aperture. A deflection field is applied, and photoelectrons from various areas are selectively made to pass through this aperture. The current passing through this aperture is amplified and recorded as a function of the location of the emitting

Table 9 - Critical Parameters for TV/Microscope Mask Inspection Systems with a 20 by 20 mm Image Tube Target

| $\delta$, μm | $NA_{min}$ | $M_{obj}$ | s, mm | $M_{tot}$ | $R_r$, μm | $\ell$, $mm^{-1}$ |
|---|---|---|---|---|---|---|
| 2 | 0.33 | 10X | 0.8 | 25X | 50 | 20 |
| 4 | 0.16 | 10X | 0.8 | 25X | 100 | 10 |
| 2 | 0.33 | 5X | 1.6 | 12.5X | 25 | 40 |
| 4 | 0.16 | 5X | 1.6 | 12.5X | 50 | 20 |

target area by a computer. Unlike the vidicon, this tube has no image storage capability and the image disappears immediately when the target illumination ceases. Consequently, although stroboscopic techniques cannot be used with this tube, it is not regimented by a raster-scan mode. The flexibility this tube offers is a random-access scanning capability that can be interfaced with a computer programmed to recognize particular features in a scan and analyze automatically these features in greater detail [28]. Electronic zoom is also possible with this tube by changing the scan amplitude or frequency. Image dissector tube are available with a matrix of 2000 by 2000 resolvable points that are scanned at the rate of 0.5 microseconds per point or 2 seconds per complete target scan. These tubes are not used in conventional raster-scanned TV applications because of their illumination requirements which are $10^3$ to $10^6$ times greater than vidicons.

The rate at which the image information can be read from these targets is a function of the time required to scan the target. The standard (U.S.) television picture contains a nominal 525 lines which are scanned 30 times a second. The advantage of using this scan rate is the economics of system construction; there is a myriad of commercial electronic equipment that is designed to operate at this scanning rate. The use of a different scanning rate or a different number of scanning lines is possible, but may involve the design and construction of special equipment.

The resolution of the TV tube is a function of the target coating, the spot size of the scanning beam for a vidicon or aperture size for image dissector, and the number of scan lines. The size of the scanning spot or aperture is a major factor in the ability to read the detail in the target image. Any defect smaller than the spot is read as if it were spread over the same area as the spot, with correspondingly less intensity. If two defects in the target image are separated by a distance of one spot diameter or less the tube signal may not drop below the threshold between the spots and they may not be recognized as separate.

A criterion for defect detection is that the spacing between successively scanned lines be equal to or smaller than the tube image of the smallest defect to be detected. This spacing can be equated to the spot size. Since the entire target area is scanned in 525 lines, the spot size or tube resolution, $R_t$, is given by

$$R_t = H/525 ,$$

where H is the dimension of the target in the direction perpendicular to the scan. The value of $R_t$ must be equal to or less than $R_r$.

Scanning the mask on a stage through successive fields of view under a microscope is accomplished most rapidly by accelerating the stage through a distance approximately one half the edge dimension of the field of view and decelerating the stage through the remaining distance to the next field of view so that it stops precisely positioned. The stage may be designed so that the natural frequency of the table moving as a rigid body on its ways as a result of elastic deformation is tuned to the applied torque of the motor and time of traverse [29]. When this tuning is accomplished the stage vibration is negligible when the table stops [29, 30].

The time required to inspect the mask is the complete cycle time multiplied by the number, N, of fields of view. The complete cycle time is the sum of the time it takes the stage to index to the next field of view and the tube cycle time, if these steps are done sequentially. A comparison is given in table 10 of the times required to scan a 3 by 3 in. (76 by 76 mm) field with a vidicon tube with a 10 by 10 mm target area and with an image dissector tube with a 25 by 25 mm target area. In making the calculations it was assumed that the optical magnification was 25X, that the stage acceleration was 4.9 $m/s^2$, and that the distances for acceleration and deceleration were equal.

The shorter of the times shown in table 10 is too long compared to the representative time of about 10 min which is typically allowed for an inspector to inspect the same mask [26]. However, it should be noted that an inspector only partially inspects the mask and relies on sampling statistics for quality control. The automatic inspection system does a 100 percent pattern inspection on all of the arrays in the mask.

Equipment has been constructed using this technology and a vidicon tube capable of counting pinholes and spots in masks which have device geometries with 2.5 μm linewidths [31, 32]. The combined optical and

Table 10 - Scan Times for Two State-of-the Art TV/Microscope Mask Inspection Systems

| Tube | s, mm | Scan time, ms | Index time, ms | Erase time, ms | Total cycle time, ms | N | Inspection time, min |
|---|---|---|---|---|---|---|---|
| Vidicon | 0.4 | 33 | 18 | 33 | 84 | 35000 | 49 |
| Image Dissector | 1.0 | 2000 | 30 | 0 | 2030 | 5600 | 190 |

electronic magnification is 250X with a 10X objective. The pinhole and spot counter operates with a fixed field of view which requires that the stage holding the mask be indexed in fixed increments. The equipment is capable of inspecting masks for wafer sizes up to 2 in. (5 cm) in diameter. In operation defects are counted as many times as they are intercepted by the TV camera scan line. The size of the smallest defect counted is a function of the smallest mask geometry. The electronics were designed so that defects are counted which are approximately 80 percent or more of the size of the smallest line width on the mask. A complete indexing cycle occurs every 8/30 s. The indexing cycle consists of 1/30 for information reading, 3/30 s for indexing and 4/30 s for complete tube erasure.

With such a system, a 100-percent inspection of a 3 by 3 in. (76 by 76 mm) mask with a field of view of 0.8 by 0.8 mm would require about 39 min. This time could be shortened to about 11 min by performing the stage indexing and erasure simultaneously in 1/30 s. This would require the use of a stroboscopic technique because the vidicon target could not be illuminated during stage indexing. Thus, the field of view could be illuminated for 10 μs or less with a strobe and stage indexing could be done during the information read out-erasure process. These modifications are within the current state-of-the-art using vidicons with more sensitive target coatings and stages that can operate and index to the required accuracy at accelerations of about 10 $m/s^2$ [30].

The speed of the system using an image dissector tube can also be improved. In principle, it is possible to construct a dissector tube using a 4 by 4 matrix of apertures, although construction of such a tube would be very expensive. This tube would scan a single field of view in 1/16 of the time now required. This would decrease the total inspection time per mask to less than 12 min. The inspection time could be reduced further by exploiting the random scanning capability and the programmable features of the image dissector tube to examine only the critical portions of the patterns on the mask. These features also would enable detailed examination of defects as they are scanned which is necessary for defect identification, but this is done by sacrificing inspection speed. These operations are normally not possible with a vidicon.

For this system to operate using either a vidicon or an image dissector tube, the signal change on going from a transparent to opaque area must be sufficient that an electronic threshold setting can distinguish between them. This places restrictions on both the signal-to-noise ratio of the TV tube and on the resultant modulation transfer function (MTF) of the microscope and TV tube. If the resultant MTF is too low the system can not distinguish between the clear and opaque areas and an erroneously low defect count may result. If the signal-to-noise ratio is not sufficiently low an erroneously high defect count may result.

The application of this technology to registration and critical dimension measurements is possible in principle. The location of a line edge to a precision of 0.25 μm increases the resolution requirements of the tube and optics. This can be accomplished by using greater optical magnifications and numerical apertures, and a larger number of scan lines on the tube target. Much more stringent requirements are also placed on knowing the precise location of the stage. The stage location can be monitored with

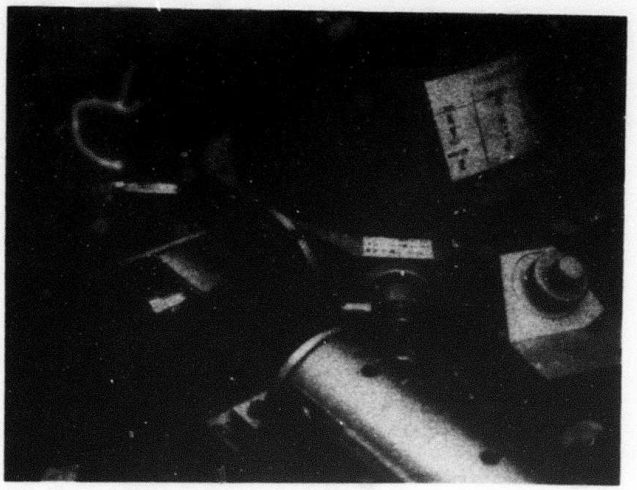


Figure 24. Polarizing laser interferometer mounted on window of scanning electron microscope.

the use of linear encoders or interferometers. The implementation of these modifications into this system can only be accomplished with a corresponding decrease in speed. (D. B. Novotny and D. R. Ciarlo*)

## 8.2. Photomask Metrology

A polarizing laser interferometer with a 1 nm displacement resolution was constructed for use with a scanning electron microscope (SEM). The SEM is being used for the accurate detection of a photomask line edge as the line is moved on a stage under a stationary electron beam. The interferometer measures the distance traversed from one line edge to the other. A helium-neon laser is the light source. Two perpendicular, linearly polarized light beams, one from the artifact mirror and one from a reference mirror located within the interferometer, overlap as they enter an analyzer. The analyzer measures the angle through which the plane of polarization of the resultant light beam rotates. An analyzer rotation of 180 degrees corresponds to an artifact mirror movement of one quarter of a wavelength. The beams reflect twice from the artifact or stage mirror and twice from the reference mirror. This doubles the interferometer sensitivity as compared to single pass interferometer systems. A photograph of the instrument, mounted on the SEM window, is shown in figure 24.

To determine the stability of the SEM stage, a mirror was mounted directly on the stage and the stage position monitored over extended periods of time. The stage used was a typical stage with x, y, z, and $\phi$ degrees of freedom and was not specifically designed for this measurement. A positional stage drift in one direction of about 20 nm/minute was observed. Superimposed on this drift were occassional sporadic stage jumps of about 100 nm.

This experimental arrangement is sensitive to differences in optical path lengths which may be caused by subtle movements of the SEM vacuum housing. Such movements can be eliminated by mounting the interferometer within the SEM vacuum chamber. In addition, a more rigid stage with fewer degrees of freedom is being obtained for use with this system. (A. W. Hartman†, J. M. Jerke†, and D. B. Novotny)

A preliminary experiment was carried out in order to determine whether a line-center to line-center (or line-spacing) measurement made on an artifact designed for calibration

---

* Lawrence Livermore Laboratory, Livermore, California 94550. Work conducted under NBS Order No. 503183.

† NBS Optics and Micrometrology Section, Optical Physics Division.

of the magnification of an SEM can also be used to calibrate a microscope equipped with a micrometer eyepiece and whether this instrument can, in turn, be used to measure a line width with desired accuracy. The artifact consisted of gold lines approximately 1-μm wide in a nickel matrix. These gold lines were separated by from 3 to 12 μm. This artifact also contained a copper line approximately 3-μm wide in the nickel matrix that was parallel to and separated by many micrometers from the gold lines. The line-width measurements were made on this copper line since it could be unambiguously identified and its edges could be more easily distinguished in the nickel matrix.

The distance between the centers of the parallel gold lines was accurately measured on the NBS line-standard interferometer [33] which related this distance to the wavelength of light with a sample standard deviation of 0.007 μm.

The experiment was performed by taking a scanning electron micrograph of the artifact which included both the gold lines and the copper line. The transparent negative of this scanning electron micrograph was placed in an optical comparator and the width of the copper line was determined to be 3.13 μm by scaling from the previously determined line separation. The sample standard deviation for this measurement was about 0.02 μm.

The width of the copper line was also measured using a microscope fitted with a filar eyepiece. The artifact was examined under bright field reflected illumination; a narrow-pass filter with a band center at 486 nm was used on the illuminator. The eyepiece was calibrated from the previously determined line separation. With the filar eyepiece the line width was found to be 3.25 μm with a sample standard deviation of 0.10 μm.

The results of this preliminary experiment indicate that line-spacing to line width measurement transfer may be possible with this type of artifact and that such a calibration method may be used for line-width measurements of metal lines in metal matrices.

(F. W. Rosberry†, J. M. Jerke†, and D. B. Novotny)

It must be stressed that the artifact used in the experiment described above differs in several significant ways from an artifact that would simulate the properties of a chromium-on-glass photomask. In the former, there is no large difference in the optical properties of the gold, nickel, or copper lines. They all reflect light well, are opaque, and are good electrical conductors. These lines are all in the same plane on the artifact surface with no edge profiles. Chromium-on-glass photomasks consist of conductive and opaque lines on a non-conductive, transparent substrate, and the line edges are distinguished by height variations.

Figure 25 shows portions of an artifact, designed for use in establishing standards for line-width measurements in the 1 to 10 μm range, which simulates the properties of such a photomask.

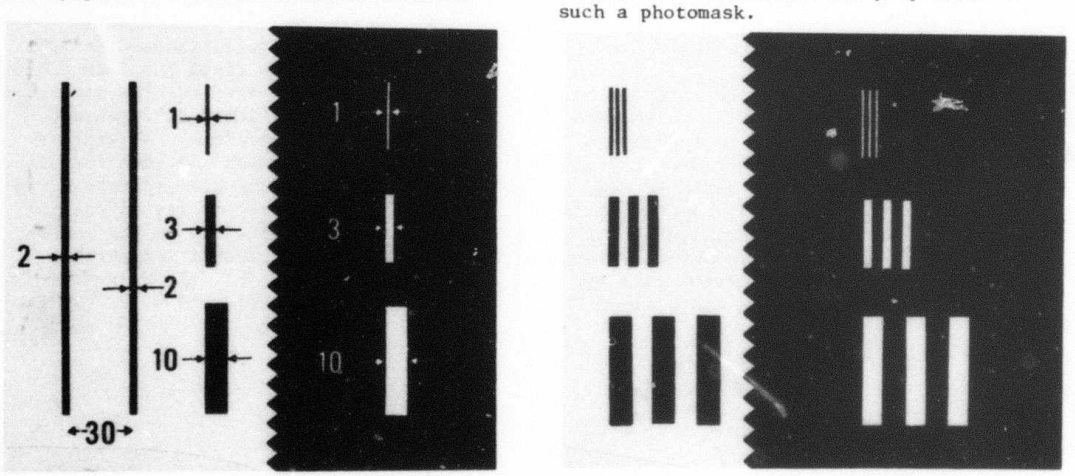



Figure 25. Typical single-line and three-line patterns on artifact for standardization of line width measurements. (Dimensions in micrometers.)

The pattern is fabricated in a film of chromium or iron oxide on a 6.4 mm thick, optically flat glass substrate coated with a thin layer of tin oxide, or other transparent, conductive material. This coating is provided in order to permit the artifact to be imaged both in the optical microscope using transmitted light and in the SEM. The flatness tolerance of the glass ($\lambda/10$ for $\lambda$ = 500 nm) is required in order that the height variation of the artifact does not cause magnification changes when the artifact is used in the SEM. The pattern includes two narrow lines which are nominally 2 μm in width and separated by about 30 μm. Adjacent to these lines are 3 opaque bars, nominally 1 μm, and 10 μm in width in a clear field. Nearby is an opaque field in which there are 3 clear lines of the same nominal widths as the opaque bars. Additional similar patterns containing two, three, and four bars and openings of each width spaced by a distance nominally equal to the line width are also included in the pattern.

The spacing between the two narrow lines can be measured to an accuracy of about ±0.02 μm by the existing NBS line standard interferometer [33]. The opaque bars on a clear background and the reversed condition of clear bars on an opaque background simulate the two conditions of contrast typically encountered in chromium and emulsion photomasks. The nominal widths of these bars were chosen to span the measurement range of interest. The multiple patterns simulate patterns found in integrated circuit masks and can be used to study the effects of adjacent bars and spaces on the measurement.

In use it is intended that the line widths on this artifact be calibrated by accurately detecting the line edges in an SEM and using an *in situ* laser interferometer to measure the line widths. A serrated edge is provided at the edge of the opaque field to assist in locating the position at which the line-width measurement is actually made to allow for accurate calibration even if the bars or openings vary in width along their length. Once calibrated, the artifact can be used to calibrate a measuring system based on an optical microscope such as a filar eyepiece or an image shearing eyepiece. (J. M. Jerke† and D. B. Novotny)

The width of a chromium line on a glass substrate was measured using both filar and image shearing eyepieces. Both bright field and dark field reflected 486 nm illumination were used. The mean values obtained for 20 measurements on the line, which was nominally 12 μm wide, under each of the above conditions are listed in table 11.

Table 11 — Comparative Measurements of the Width of a Chromium Line on Glass

| Eyepiece | Illumination | |
|---|---|---|
| | Bright Field | Dark Field |
| Filar | 11.76 μm | 11.06 μm |
| Image Shearing | 11.87 μm | 11.83 μm |

The sample standard deviation in each case was about 0.08 μm. The difference between the widths measured using the filar and image shearing eyepieces with bright field illumination is less than two sample standard deviations while the difference measured with dark field illumination is greater than nine sample standard deviations. If the bright field and dark field measurements are compared for the same type of eyepiece, a significant difference occurs for the filar eyepiece. No explanation for this phenomenon has been formulated, but these discrepancies represent typical measurement discrepancies currently found for this size pattern in the photomask and integrated circuit industries.

(F. W. Rosberry†, J. M. Jerke†, and D. B. Novotny)

# 9. EPITAXIAL LAYER THICKNESS

## 9.1. Transient Capacitance Methods

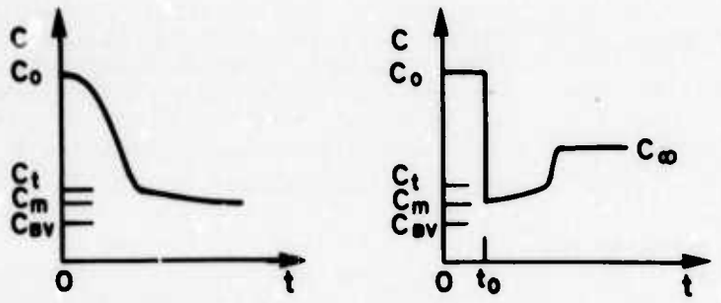
An analysis was performed to study the limitations of the ramp-voltage and step-relaxation methods for measuring epitaxial layer thickness (NBS Spec. Publ. 400-4, pp. 51-53). Both of these methods utilize the transient capacitance of a metal-oxide-semiconductor (MOS) capacitor or a metal-photoresist-semiconductor (M(PR)S) capacitor (NBS Spec. Publ. 400-12, p. 26). Potential limitations arise for three reasons: (1) voltage breakdown may occur when the edge of the depletion region is in the epitaxial layer, (2) the steady-state depletion width in inversion may be greater than the layer thickness, and (3) the carrier lifetime in the depletion region may be so short that no transient can be observed. In discussing these limitations it is necessary to ask not only whether a real thickness measurement can be made but also to inquire under what circumstances an apparent measurement might be mistaken for a real thickness measurement. It is assumed that the voltage available to bias the capacitor is sufficient to drive the depletion region into the substrate.

The ideal capacitance-time characteristics (case 1) for the ramp-voltage and step-relaxation methods are illustrated in figure 26. In the figure, $C_o$ is the steady-state capacitance in accumulation (the oxide capacitance, $C_\infty$ is the steady-state capacitance in inversion, $C_t$ is the capacitance when the depletion edge is at the layer-substrate interface, (the value used to calculate the epitaxial layer thickness), $C_m$ is the capacitance which corresponds to the maximum applied bias voltage (deep depletion region), and $C_{BV}$ is the capacitance which corresponds to the breakdown voltage. The voltage step in the step-relaxation method is applied at a time, $t_0$. Note that for both methods a discontinuity in the slope of the C-t curves occurs at $C = C_t$ and that $C_{BV}<C_m<C_t<C_\infty$.

First consider the effects of voltage breakdown under two conditions which might occur: case 2, in which breakdown occurs after the depletion edge has gone beyond the layer-substrate interface but before the maximum bias voltage is reached ($C_m<C_{BV}<C_t$), and case 3, in which breakdown occurs before the depletion edge has reached the layer-substrate interface ($C_t<C_{BV}$). In case 2, illustrated in figure 27, the slope discontinuity can still be observed and the measurement made by both methods; in the ramp-voltage method there is a finite slope between $C_t$ and $C_{BV}$, but the capacitance is constant after breakdown occurs. In case 3, illustrated in figure 28, measurement is not possible because the capacitance $C_t$ is not reached. This condition can be identified by the flat response immediately following the slope discontinuity in the ramp-voltage method (fig. 28a) and by the absence of a slope discontinuity between the minimum and $C_\infty$ in the step relaxation transient (fig. 28b). Measurements of the step response of a specimen were made under conditions which appear to correspond to case 2. In these instances there appeared to be a transition from the ideal case to case 2 as the voltage in inversion was made more negative. Case 3 was simulated using an MOS capacitor fabricated on a bulk *n*-type silicon slice having a nominal 0.1 Ω·cm resistivity. Response curves similar to those in figure 28 were observed in this experiment.

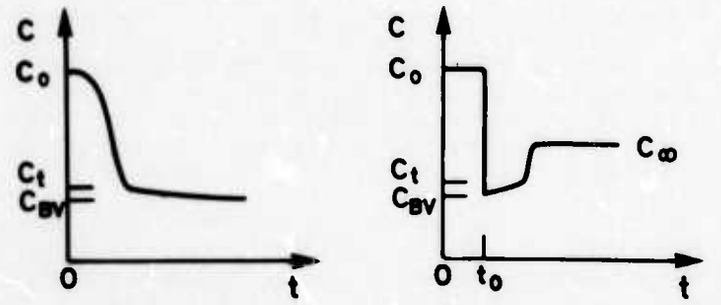
Consider now case 4 in which the steady state depletion width exceeds the epitaxial layer thickness. This case occurs if the dopant density is sufficiently low that the depletion region extends into the substrate. If the dopant density in the substrate is very large, the depletion region can penetrate only a very small distance into the substrate so that $C_\infty \simeq C_t$. However, if the dopant density in the substrate is not very large, the depletion region may penetrate an appreciable distance and $C_\infty < C_t$. The transient in the ramp-voltage method is not affected by the position of the depletion edge; the slope discontinuity at $C_t$ occurs whether $C_t>C_\infty$ or $C_t<C_\infty$. However, as shown in figure 29, the step-relaxation transient exhibits no slope discontinuity between the minimum and $C_\infty$. Although $C_\infty \simeq C_t$ in most wafers of practical interest, it is not possible to distinguish the occurrence of case 4 unambiguously from the occurrence of case 3 when using the step-relaxation method. Therefore this method is not recommended for use when no slope discontinuity is observed.

The question of measurability of a particular specimen can be resolved readily with the help of figure 30 if one has or can assume some prior knowledge of layer resistivity



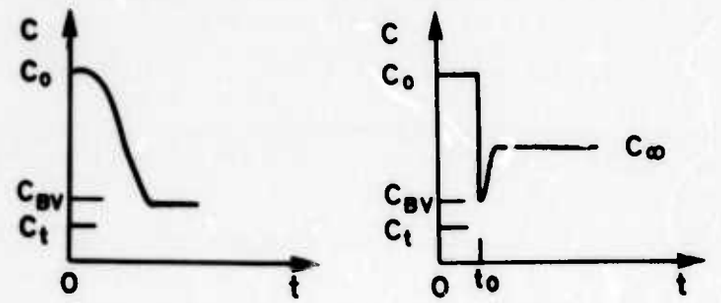

a. Ramp-voltage method. b. Step-relaxation method.

Figure 26. Ideal capacitance-time characteristics for an MOS capacitor on a thin epitaxial layer.




a. Ramp-voltage method. b. Step-relaxation method.

Figure 27. Capacitance-time characteristics for an MOS capacitor on a thin epitaxial layer when voltage breakdown occurs at voltages less than the maximum applied bias voltage but greater than the bias voltage which corresponds to the depletion edge at the layer-substrate interface.




a. Ramp-voltage method. b. Step-relaxation method.

Figure 28. Capacitance-time characteristics for an MOS capacitor on a thin epitaxial layer when voltage breakdown occurs at voltages lower than the bias voltage which corresponds to the depletion edge at the layer substrate interface.

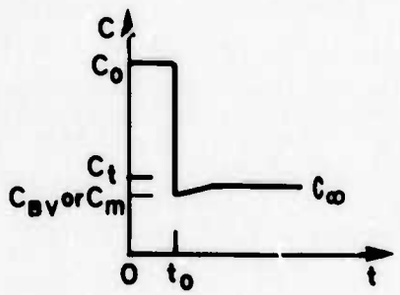



Figure 29. Step-relaxation capacitance-time characteristic for an MOS capacitor on a thin epitaxial layer when the steady state depletion width equals or exceeds the layer thickness.

and thickness. This knowledge can be very approximate and still be useful. In figure 30, breakdown normally occurs in the layer in those specimens whose dopant density and layer thickness are such that they can be represented by a point above the solid line [34]. Such specimens cannot be measured by either method. The broken line in figure 30 represents the case where the layer thickness is equal to the steady state depletion width

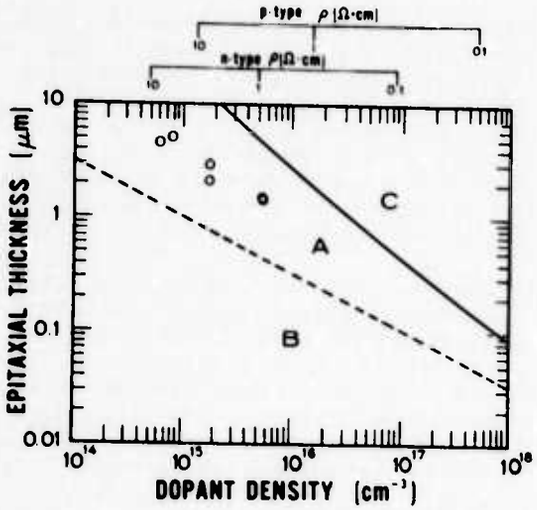



Figure 30. Plot of epitaxial layer thickness and dopant density showing regions where thickness can be measured by both the ramp-voltage and step-relaxation methods (A), by only the ramp-voltage method (B), and by neither of these methods (C). (O: measured specimens.)

so that $C_\infty = C_t$ [35]. Specimens whose dopant density and layer thickness are such that they can be represented by a point below the broken line fall in case 4 and should not be measured by the step-relaxation method.

Whether carrier lifetime presents a limitation depends largely on the response time of the instrumentation being used to make the measurement. When the carrier lifetime is very short, the capacitance transient is very fast so that only the steady-state capacitance-voltage curve can be observed.

In some cases, cooling the specimen can slow the response time to the extent that the capacitance transient can be observed (NBS Spec. Publ. 400-4, pp. 51-53) [36]. However, it appears most likely that the measurement is not possible when the lifetime is so short that no transient response can be observed. The effect of lifetime does not appear in figure 30.

The results of the analysis are summarized in table 12. Several words of caution need to be added. First, for lower dopant densities, breakdown may occur at shallower depths than indicated by the solid line in figure 30 because of peripheral breakdown effects [37]. Second, the step response of bulk specimens may exhibit significant changes in slope during the course of the transient, but these are generally different from the distinct break which occurs at a layer-substrate interface. Third, the methods presented depend on the response curves having a finite slope in the substrate in the absence of breakdown. More heavily doped substrates tend to have flatter response curves which may make it difficult to distinguish between slope discontinuities at $C_t$ and $C_{BV}$. However, even for very heavy doping, sidewall spreading of the depletion layer should cause the slope to be finite. Fourth, the analysis, although carefully considered, has been only partially substantiated by experimental data. The specimens for which data have previously been reported (NBS Spec. Publ. 440-4, pp. 51-53) are shown as plotted points on figure 30. Note that they all correspond to the ideal case which is the most easily measured.

(R. L. Mattis and M. G. Buehler)

Table 12 - Summary of Analysis of Limitations of Transient Capacitance Methods for Measuring Epitaxial Layer Thickness

| Case | Breakdown Condition | Depletion Condition | Lifetime Condition | Measurement Possible By |
|---|---|---|---|---|
| 1 | $C_{BV}<C_m<C_t$ | $C_\infty>C_t$ | Long Lifetime | Either Method |
| 2 | $C_{BV}<C_t$ | $C_\infty>C_t$ | Long Lifetime | Either Method |
| 3 | $C_t<C_{bV}$ | $C_\infty>C_t$ | Long Lifetime | Neither Method |
| 4 | $C_{BV}<C_\infty$, $C_m<C_\infty$ | $C_\infty \leq C_t$ | Long Lifetime | Ramp-Voltage Method |
| 5 | any | any | Short Lifetime | Neither Method |

# 10. WAFER INSPECTION AND TEST

## 10.1. Flying-Spot Scanner

Additional modifications were made to the optical flying-spot scanner to enhance its usefulness. Additions and changes to the optical system are illustrated in figure 31. The original laser (NBS Spec. Publ. 400-8, pp. 34-36) is now used only for 1.15 μm service, and an additional laser, shown on the left, has been added for dedicated 0.633 μm operation. Scanning is shifted between these two wavelengths by moving mirror $M_3$ which is mounted on a slide. As shown in the figure, $M_3$ blocks the beam from the 1.15 μm laser and inserts the 0.633 μm beam into the light path between the fixed mirror $M_2$ and the first scanning mirror V; for 1.15 μm operation, $M_3$ is withdrawn from the light path to the dotted position in the figure. In addition, a half-wave plate has been added to the light path of the 1.15 μm beam to allow the polarization plane of the radiation to be rotated and the intensity of the reflected-light signal to be adjusted.

The video amplifiers between the scanned specimen and the display screen were replaced by custom designed direct-coupled amplifiers when it was discovered that under certain conditions the former oscillated and produced harmonics at frequencies close to the laser-mode-beat frequencies and so obscured these high-frequency measurements. As an additional benefit, the present circuit permits one to obtain the response of the specimen to laser-mode-beat modulated light (NBS Spec. Publ. 400-12, p. 27) simultaneously with the response to unmodulated light. These two responses may be electronically summed to present a composite response map on the display screen. In addition, a high-impedance specimen probe was designed and added to the system to couple the scanner to MOS circuits. It features an input impedance of 22 MΩ in shunt with a 3.1 pF capacitance, and it is both direct-coupled and wide-band in consonance with the amplifiers which follow it.

Attempts to vary the light from the 0.633 μm laser by modulating the laser tube current were successful, and a modulator was constructed which yields a 10 percent or greater modulation of the light for frequencies between dc and 100 kHz. This is expected to enable the instrument to perform stroboscopic scanning measurements on integrated circuits to follow the internal information flow, and locate defects which impede this flow.

Several integrated circuits were observed with the scanner in order to gain further information regarding its operation. Most of the observations were made using only the two supply bus contacts; the display-screen signal was obtained by sensing, via a resistor, changes in the bus current. This signal was combined with the one from the reflected-light circuit to produce on the screen the electrical response of the integrated circuit superimposed on a map of the surface metallization.

One of the circuits studied was a bipolar, junction-isolated, two-input, NAND gate (7438). The electrical response of the circuit to the scanning light spot arises in

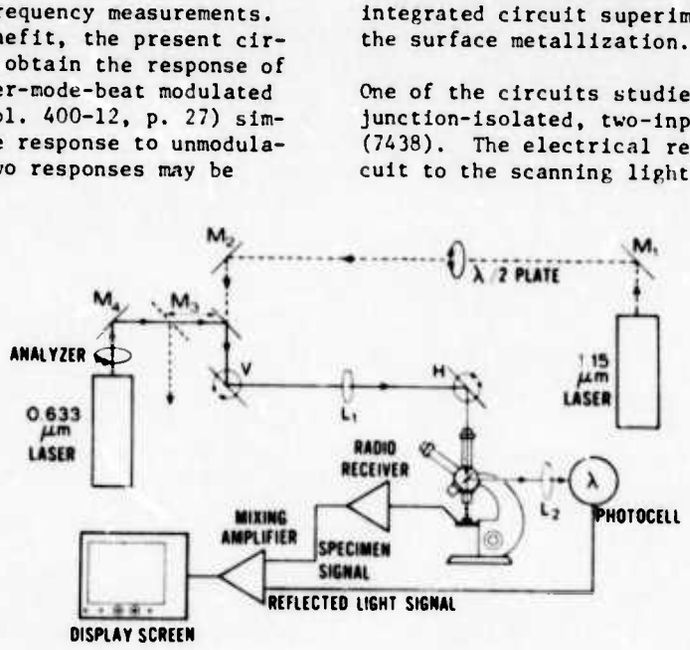



Figure 31. Pictorial diagram of light and signal paths of dual-laser flying-spot scanner.

the following way: current injected into the base of a transistor, whether injected across a junction or photogenerated within the base region, is amplified by the transistor if the transistor is biased appropriately. This amplified current is taken from the supply bus. Thus, transistors operating in the active region, in which there is significant small signal current gain, are readily identified as they show a large photoresponse to 0.633 μm light and consequently produce an image on the display screen. Changing the state of the NAND circuit yields a new map of the active elements.

The 0.633 μm radiation penetrates silicon to a depth of only 1 or 2 μm at room temperature, but the 1.15 μm light penetrates quite deeply; the silicon is almost transparent at the latter wavelength. As isolation diffusions in integrated circuits are commonly much deeper than a few micrometers, they are not seen on the monitor screen as readily using 0.633 μm light as the active regions of the transistor which generally are within a few micrometers of the surface. However, the isolation diffusions of the NAND gate were easily displayed using 1.15 μm radiation.

Additional information about the construction, as well as the operation, of the integrated circuit is provided by high-frequency measurements using laser mode beats: for example, diffusions surrounding the bonding pads at the periphery of the die were detected. Thus, comparing observations made using all of these available scanning techniques can yield not only information about the electrical behavior of the integrated circuit, but also information about the sequence of steps employed in its fabrication.

As a beginning in the use of the scanner for MOS integrated circuits, two complementary transistors in a silicon-on-sapphire 4007 (dual complementary pair plus inverter) were connected to form an inverter stage and scanned with 0.633 μm light. As for the bipolar NAND gate work described above, the signal for the display screen was obtained from the supply voltage bus. The operation of the circuit was changed by changing the bias conditions, and one could readily distinguish which were the conducting transistors for each of the bias conditions.

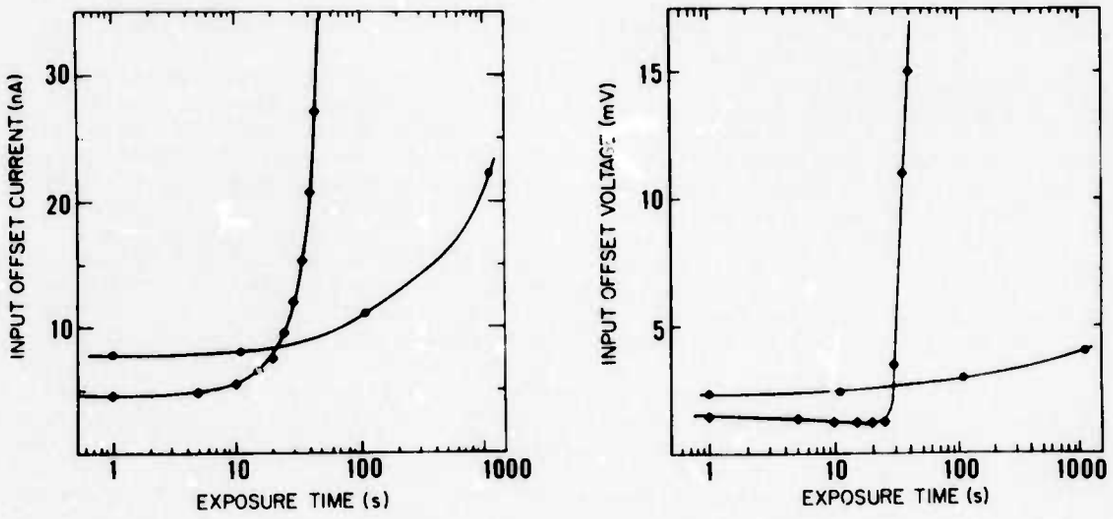
(D. E. Sawyer and D. W. Berning)

## 10.2. Scanning Electron Microscopy — Electron-Beam Induced Damage

The well controlled low-energy electron beam used by the scanning electron microscope (SEM) is a potential source of damage to microelectronic devices under examination. Because an electron energy of approximately 200 keV or greater is necessary to cause displacement damage in silicon, the bulk properties of the devices being examined are usually unchanged at typical electron accelerating voltages. However, the electron energy deposition in the device materials through ionization processes may result in changes in the surface oxide properties. The effect of this energy deposition on the degradation of device electrical parameters has been noted for both bipolar [38-42] and MOS [42-49] devices. To illustrate the effects of exposure to SEM beams, the electrical parameters of a digital bipolar circuit, a linear bipolar circuit, and an MOS circuit were monitored as a function of SEM operating conditions.

The first integrated circuit to be examined was a digital bipolar inverter, the 7404. Of the six inverters on the 7404 chip, only the characteristics of one were monitored. Measurements were made to determine if the device met the manufacturer's minimum specifications for both high-and-low-level outputs after exposure in an SEM operating with an electron beam energy, $E_B$, of 20 keV at a beam current, $I_B$, of 100 pA scanning an area, $A_s$, of 0.02 $cm^2$. No change in electrical characteristics was detected after a 1000 s exposure with all leads grounded. The same device was then exposed for 1000 s with a collector supply voltage of 4.75 V and an input voltage of 2.0 V and again for 1000 s with the same collector supply voltage but an input voltage of 0.8 V. No change in electrical characteristics was observed after either exposure. An additional 1000 s exposure with a beam current of 1 nA produced no measureable damage. This particular device appears insensitive to changes in surface oxide properties and is not susceptible to SEM damage. Identical results were obtained with other samples of this device type.

A linear bipolar device, a 741 operational amplifier, was the next integrated circuit examined. The input offset current, $I_{os}$, and the input offset voltage, $V_{os}$, were monitored as a function of exposure time in




a. Input offset current.

b. Input offset voltage.

Figure 32. Characteristics of 741 operational amplifiers as a function of exposure time in a 20 keV beam of a scanning electron microscope. (●: Device not biased during exposure; ◆: Device biased during exposure.)

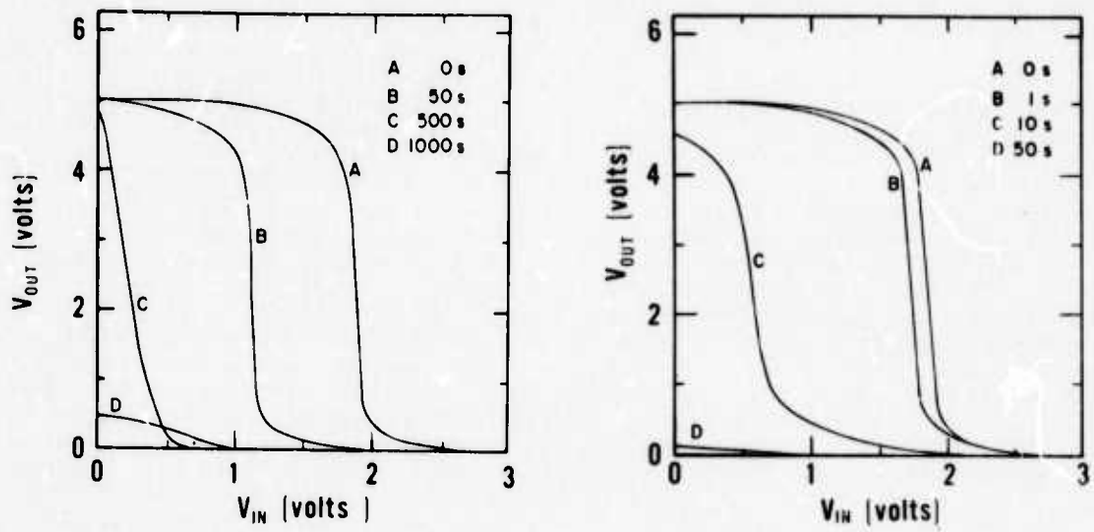
the SEM. One sample was scanned with the leads grounded while another had +15 V applied to the positive collector supply terminal and to the non-inverting input and -15 V applied to the negative collector supply terminal and to the inverting input during exposure. The SEM operating conditions were:

$A_s$ = 0.03 $cm^2$, $I_B$ = 100 pA. $E_B$ = 20 keV.

The changes in $I_{os}$ and $V_{os}$ as a function of exposure time in the SEM beam are shown in figure 32. With bias applied during exposure, both $I_{os}$ and $V_{os}$ exceeded the manufacturer's maximum specifications after an exposure of less than 100 s. Additional samples were examined and yielded similar results.

The third integrated circuit type examined was a C-MOS 4007, a dual complementary pair plus inverter. The particular circuit used was fabricated using silicon-on-sapphire technology. The inverter characteristics were first monitored as a function of SEM voltage. No change in the inverter characteristics was observed when a single circuit with leads floating was exposed successively to 2.5, 5.0, and 10.0 keV beams for 1000 s intervals with $I_B$ = 100 pA and $A_s$ = 0.02 $cm^2$. Changes, as shown in figure 33, were observed when the circuit was exposed to a 20.0 keV beam with the same values of $I_B$ and $A_s$. Measurements were made after exposure of the circuit for 50, 500, and 1000 s with the leads floating. Significant shifts were observed after each exposure, and the device was inoperative after the 1000 s exposure. Measurements were also made after exposure of a different circuit of the same type for 1, 10, and 50 s with +5 V applied to both the drain and input terminals. Severe shifts in characteristics occurred after the 10 s exposure and after 50 s the device was inoperative. As is the case with exposure of these circuits to gamma radiation, the degradation of the CMOS inverter characteristics is more severe when exposed with voltages applied.

The electrical parameters of microelectronic devices are usually sensitive to changes in the oxide characteristics of those oxide films near the active silicon regions. For an MOS device such as the 4007, the ionizing effects of the SEM electron beam can be measured in terms of the energy deposited in the gate oxide. In order to facilitate the comparison of SEM electron beam ionization damage with the effects of other ionizing sources, the radiation dose unit, the rad which is defined as the amount of radiation which deposits 100 ergs of energy per gram




a. Circuit not biased during exposure.

b. $V_{DD} = V_{IN} = +5$ V during exposure.

Figure 33. Characteristics of C-MOS 4007 circuit after various exposures to a 20 keV beam of a scanning electron microscope.

of irradiated material, is ordinarily employed (1 rad = $10^{-2}$ J/kg).

If normal beam incidence and uniform electron flux over the rastered area is assumed and the device structure above the critical oxide is known, the radiation dose levels in the pertinent surface oxides for a device exposed to the SEM electron beam can be calculated from

$$\text{Dose [rads(SiO}_2\text{)]} = 100\,\frac{I_B E_B t f_D}{A_s T_{ox}}, \quad (11)$$

where t is the scan time in seconds, $f_D$ is the fraction of incident energy deposited in the oxide, $T_{ox}$ is the oxide thickness in micrograms per square centimeter, and the remainder of the symbols have been defined earlier. The fraction $f_D$ is the area under the depth-dose curve [50] for that portion of the total penetration distance subtended by the oxide after proper account is taken of the fraction of energy backscattered, $f_B$, assumed for the present calculations to be 0.1 [51].

The dose accumulated in the gate oxide of the 4007 circuits was calculated from eq (11). The structure above the 100 nm gate oxide consisted of an aluminum film approximately 1.0 μm thick and a silicon dioxide overcoat approximately 0.6 μm thick. The accumulated dose per second of exposure time is given in table 13 as a function of beam energy for $I_B$ = 100 pA and $A_s$ = 0.02 cm$^2$. The experimental observation of no degradation at 2.5, 5.0, and 10.0 keV is in agreement with the calculations. A 71 s exposure of 20 keV electrons under these operating conditions results in a dose of $10^6$ rads($SiO_2$), a suf-

Table 13 — Dose Accumulated in Gate Oxide for 1 Second SEM Exposure

| $E_B$, keV | $f_D$ | Dose, rads($SiO_2$) |
|---|---|---|
| 2.5 | 0.0 | 0.0 |
| 5.0 | 0.0 | 0.0 |
| 10.0 | 0.0 | 0.0 |
| 15.0 | 0.012 | $3.8 \times 10^3$ |
| 20.0 | 0.033 | $1.4 \times 10^4$ |
| 30.0 | 0.020 | $1.3 \times 10^4$ |

ficient dose to cause significant electrical parameter changes for many classes of devices.

The SEM operating parameters utilized in this report are typical of those used in SEM topographical examinations of devices. It is apparent that for some classes of devices little or no electrical parameter degradation occurs. However, for others, even a brief examination can be destructive. SEM induced degradation is a function of accelerating voltage, beam current, scanned area, exposure time and bias voltages applied to the device under test. (K. F. Galloway, W. J. Keery, and K. O. Leedy)

## 10.3. Automated Scanning Low Energy Electron Probe

The initial goals of the investigation of the automated scanning low energy electron probe (ASLEEP) (NBS Spec. Publ. 400-12, p. 28) are to construct the instrument and demonstrate proof of principle by application of the instrument to the determination of the uniformity of oxide films. The effort encompasses research in electron gun design, fabrication, and test as well as computer interfacing and software generation.

Basically, ASLEEP utilizes a low energy electron beam under computer control to measure surface potential. A simplified block diagram is shown in figure 34. The instrument has potential usefulness in areas ranging in complexity from incoming wafer acceptance to integrated circuit diagnostics.

In preparation for the alignment and testing of the electron gun for the ASLEEP system, a uniform aluminum grid on a silicon dioxide substrate has been fabricated. This grid is used to measure the linearity of the beam positioning circuitry and, as the computer programming progresses, should allow calculation of a computerized correction factor to remove beam steering errors. The system response to one line of this grid can also provide an estimate of the electron beam spot size.

In order for the instrument to provide absolute surface potential measurements, a calibrated standard target is required. Since the work functions of the low index planes of tungsten have been exhaustively studied, a standard target was fabricated from tungsten ribbon using recrystallization techniques [52-54]. When this single crystal reference target is mounted on a vacuum manipulator, either the reference or the specimen under test may be placed in front of the electron gun.

The computer control system has been acquired and the necessary software and interface projects are underway.

(W. C. Jenkins* and G. P. Nelson*)

---

* Work conducted at the Naval Research Laboratory, Washington, D. C. 20375 under NBS Order No. 501718. NBS contact for additional technical information: K. F. Galloway.

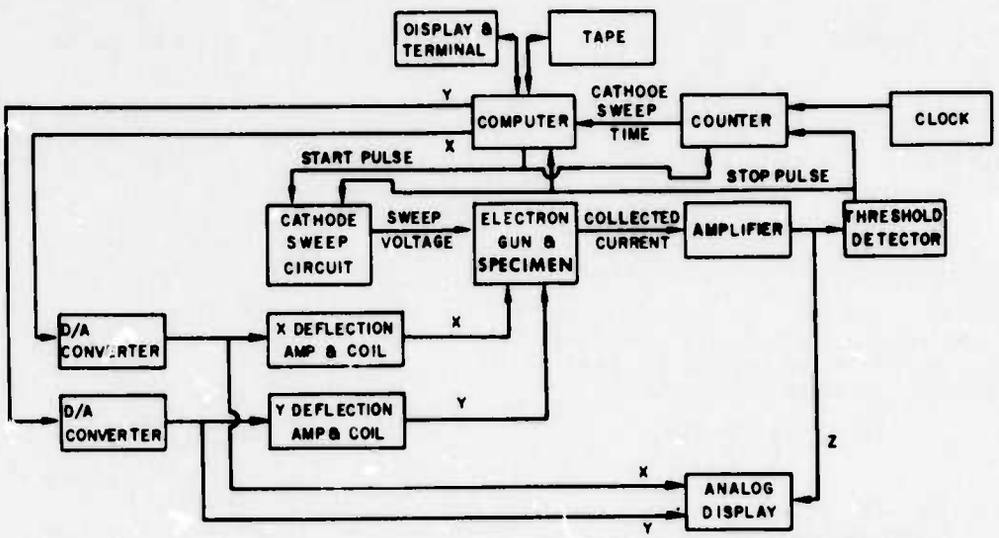



Figure 34. Block diagram of automated scanning low energy electron probe.

# 11. INTERCONNECTION BONDING

## 11.1. In-Process Bond Monitor

The study of the uniform beam model for motion of an ultrasonic bonding tool (NBS Spec. Publs. 400-8, pp. 37-39, and 400-12, pp. 29-30) was extended to include the force at the tool tip during the bonding operation. This force, $F(\ell,t)$ is related to the third spatial derivative of the vibration amplitude at the tool tip by

$$F(\ell,t) = -EI\, Y'''(\ell,t) ,$$

where EI is the flexural rigidity of the tool and $\ell$ is the tool extension below the horn. If the tool is driven sinusoidally at the horn, the boundary conditions to be used are

$$Y(0,t) = a\sin\omega t,\ Y'(0,t) = 0,\ Y''(\ell,t) = 0, \text{ and } Y'''(\ell,t) = -\frac{F(\ell,t)}{EI} , \tag{12}$$

where a is the vibration amplitude of the tool at the transducer horn (x = o) and $\omega$ is the vibration frequency.

The general solution to the equation which describes the motion of the tool in space and time (NBS Spec. Publ. 400-4, pp. 65-66) is

$$Y(x,t) = B_1\sinh(qx) + B_2\cosh(qx) + B_3\sin(qx) + B_4\cos(qx), \tag{13}$$

where $q = (\rho A\omega^2/EI)^{1/4}$, $\rho$ is the volume density of the tool material, and A is the cross sectional area of the tool. Making use of eqs (12) in eq (13) and introducing the dimensionless variables $Z = q\ell$, $N = x/\ell$, the solution may be shown to be in the form

$$\begin{aligned} Y(N,t) = {} & \frac{a\sin\omega t}{2D(Z)}\left\{A(Z)[\sin(NZ) - \sinh(NZ)] + B^{+}(Z)\cosh(NZ) + B^{-}(Z)\cos(NZ)\right\} \\ & + \frac{F(\ell,t)}{2q^3EI\,D(Z)}\left\{[\cosh(Z) + \cos(Z)][\sin(NZ) - \sinh(NZ)]\right. \\ & \left. + [\sinh(Z) + \sin(Z)][\cosh(NZ) - \cos(NZ)]\right\}, \end{aligned} \tag{14}$$

where

$$D(Z) = 1 + \cosh(Z)\cos(Z) ,\ A(Z) = \sin(Z)\cosh(Z) + \cos(Z)\sinh(Z), \text{ and}$$

$$B^{\pm}(Z) = D(Z) \pm \sinh(Z)\sin(Z).$$

It should be noted that the first term of eq (14) is just the solution of the driven uniform beam in the unloaded phase of operation, $Y_o(N,t)$. Hence, in the limit as the tool tip-wire force goes to zero, Y(N,t) approaches the previously determined solution (NBS Spec. Publ. 400-8, pp. 37-39).

The solution, Y(N,t), can be simplified to

$$Y(N,t) = Y_o(N,t) + F(\ell,t)\Phi(N),$$

where $\Phi(N)$ is defined as

$$\phi(N) = \frac{1}{2q^3EI\ D(Z)}\{[\cosh(Z) + \cos(Z)][\sin(NZ) - \sinh(NZ)]$$

$$+ [\sinh(Z) + \sin(Z)][\cosh(NZ) - \cos(NZ)]\}.$$

At the $i$th node, the unloaded beam solution, $Y_o(N_{oi},t)$ is zero so the solution at the node becomes

$$Y(N_{oi},t) = F(\ell,t)\phi(N_{oi}). \tag{15}$$

From eq (15) it can be seen that the temporal evolution of the tool vibration amplitude at a nodal position of the unloaded beam provides direct insight into the temporal evolution of the force at the tool tip during the bonding operation. An elucidation of this force can provide information about the mechanism of ultrasonic bonding particularly in regard to the ultrasonically induced plasticity of the aluminum wire and the relation of this plasticity to the bonding mechanism.

At the tool tip, $N = 1$, the solution becomes

$$Y(1,t) = \frac{a\sin\omega t}{D(Z)}\left[\cosh(Z) + \cos(Z)\right] + \frac{F(\ell,t)}{q^3EI\ D(Z)}\left[\cosh(Z)\sin(Z) - \cos(Z)\sinh(Z)\right].$$

Hence, the amplitude at the tool tip also provides a measure of the force at the tool tip during bonding.

(J. H. Albers)

# 12. HERMETICITY

## 12.1. Dry Gas Gross Leak Procedures

The limiting factor in dry gas leak test procedures is the rapid depletion of the gas from the package interior which causes nondetection of large leaks. A Knudsen expansion-differential sensing method was devised previously to eliminate this factor (NBS Spec. Publs. 400-4, p. 70, and 400-8, p. 42). Another procedure has now been considered as a possibility for extending the range of currently available instruments by effectively reducing the delay between the back pressurization phase and the detection of tracer gas which has penetrated the package. This procedure employs a rapid gas cycling technique.

In addition to reducing the delay time, the procedure is intended to provide controlled environmental conditions so that a quantitative relationship between true and measured leak value can be reasonably well derived while maintaining the testing time at an acceptably low value. While the method may be applied to either the helium leak detector or the radiotracer apparatus, the description which follows is for the former.

A single chamber doubles for pressurization and detection. Dwell time is minimized by rapid gas expansion, and excess helium is diminished by dilution. The gas handling circuit is shown schematically in figure 35; standard symbols [55] are used to indicate the components. All valves are quick acting. The ratio, r, of the ballast volume, $B_1$ or $B_2$, to the volume of the chamber, A, in which the devices to be tested are placed should be 100 or more. Helium is introduced into chamber A to the desired pressure for a specified time of the order of seconds. The chamber is then vented first to the atmosphere and then into the ballast tank $B_1$ in a continuous sequence of about 1 s duration to reduce the helium gas pressure surrounding the test specimens to a pressure of 1/r atm. Nitrogen gas (or dry air) is then introduced into chamber A to dilute the remaining helium within about 1 s by a factor equal to the product of the nitrogen pressure, $P_n$ (in atmospheres), and the ratio r. The mixture in chamber A and associated lines is again vented to atmosphere and expanded, first into $B_1$ and then into $B_2$. Thus, the pressure in chamber A is reduced to $1/r^2$ atm by the double expansion. The partial pressure of helium in the chamber is $1/P_n\ r^3$ atm.

At this time, with valves 7 and 8 closed and valve 2 opened, any helium in the chamber remaining from the expansion and dilution sequences or leaking from the specimen interiors would pass through the fixed leak, FL, into the helium leak detector to give an indication. When the pressure in chamber A is further reduced by the mechanical pump to low enough value, valve 1 may be opened and valve 6 closed for unrestricted passage into the leak detector.

The fixed leak and the final expanded pressure are of such values that the gas flow rate into the leak detector does not cause the detector internal pressure to rise above operational limits. The maximum allowable helium concentration in chamber A is then set by the ratio of the leak detector limit of indication to the value of the fixed leak conductance. The minimum detectable indicated leak rate at any instant is approximately the product of the fixed leak conductance and the partial pressure of helium in the mixture surrounding the sample. This minimum detectable signal falls off with a time constant determined by the pumping speed at the chamber and the chamber volume.

To relate the measured leak rate, $Q_m$, to the leak size, L, it is necessary to calculate the pressure in the specimen package at the time of measurement. Since the test is concerned with the measurement of gross leaks,

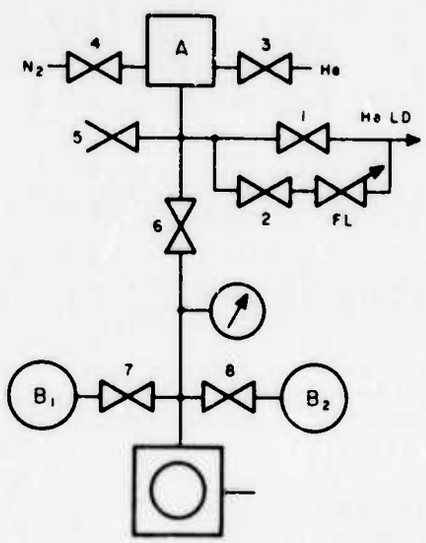



Figure 35. Gas handling circuit for rapid gas cycling technique for measurement of gross leaks.

it is assumed that gas transport is essentially described by laminar viscous flow; under the conditions selected in the sequences, diffusive flow is not a factor.

In the first step, the specimens are back pressurized. The final internal pressure $P_1$ is

$$P_1 = \gamma_1 P_t = P_t \frac{1 - \left(\frac{P_t - P_0}{P_t + P_0}\right) \exp(-T_1/\tau_1)}{1 + \left(\frac{P_t - P_0}{P_t + P_0}\right) \exp(-T_1/\tau_1)},$$

where $P_t$ is the helium pressure during pressurization, $T_1$ is the pressurization time, $P_0$ is atmospheric pressure, the time constant $\tau_1 = VP_0^2/2P_tL$, and V is the interior volume of the test package. When the gas is expanded, the internal pressure falls to

$$P_2 = \delta_1 P_1 = P_1 \left(1 + \frac{\gamma_1 t_1}{2\tau_1}\right)^{-1},$$

where $t_1$ is the time interval of gas venting and expansion. Recharging with nitrogen causes the internal pressure to increase to

$$P_3 = \gamma_2 P_n = P_n \left[\frac{1 - \left(\frac{1 - \gamma_1\delta_1}{1 + \gamma_1\delta_1}\right) \exp(-T_2/\tau_2)}{1 + \left(\frac{1 - \gamma_1\delta_1}{1 + \gamma_1\delta_1}\right) \exp(-T_2/\tau_2)}\right],$$

where $T_2$ is the recharging time, $P_n$ is the recharging pressure, and the time constant $\tau_2 = VP_0^2/2P_nL$. Finally, the gas is vented, subjected to a double expansion, and opened to the leak detector. The internal pressure at the time of measurement is

$$P_4 = \delta_2 P_3 = P_3 \left(1 + \frac{\gamma_2 P_n t_2}{2P_t \tau_1}\right)^{-1},$$

where $t_2$ is the time interval for this step. The partial pressure of helium in the package is now $(P_1 - P_0)P_2/P_1P_3$ so that the measured leak rate is

**Table 14 — Typical Examples of Leak Rates Measured using Rapid Gas Cycling Gross Leak Test**

| $\tau$ | $\gamma_1$ | $\delta_1$ | $\gamma_2$ | $\delta_2$ | $Q_m/L$ |
|---|---|---|---|---|---|
| 1 | 1 | 0.67 | 0.947 | 0.175 | 0.39 |
| 10 | 0.6 | 0.77 | 0.537 | 0.789 | 2.6 |
| 100 | 0.25 | 0.99 | 0.257 | 0.987 | 0.31 |

Note: $P_t = P_n = 5$ atm; $T_1 = 10$ s; $t_1 = 1$ s; $T_2 = 2$ s; $t_2 = 10$ s; $\tau = \tau_1 = \tau_2 = V/10$ L.

$$Q_m = \frac{P_1 - P_0}{P_1} \frac{P_2}{P_3} \left(\frac{P_4}{P_0}\right)^2 L. \qquad (16)$$

Eq (16) can also be written

$$Q_m = (\gamma_1\alpha_1 - 1)\, \delta_1\delta_2^2\gamma_2\alpha_2\, L,$$

where $\alpha_1 = P_t/P_0$ and $\alpha_2 = P_n/P_0$.

To illustrate this result, calculations were carried out for the case where $P_t = P_n = 5$ atm, $T_1 = 10$ s, $t_1 = 1$ s, $T_2 = 2$ s, and $t_2 = 10$ s. For these conditions $\tau_1 = \tau_2 = \tau = V/10$ L where V is given in cubic centimeters and L is given in atmosphere cubic centimeters per second. Results for time constants of 1, 10, and 100 s are given in table 14. The calculations show that for these conditions a package with a 1 $cm^3$ internal volume and a $10^{-1}$ atm·$cm^3$/s leak would evidence a measured leak rate about 0.4 times the leak size while a package with a $10^{-2}$ $cm^3$ internal volume and a $10^{-5}$ atm·$cm^3$/s leak would evidence a measured leak rate about 0.3 times the leak size, all within the limits of typical apparatus. For the cases studied, the helium remaining from the expansion and dilution sequences is negligible compared with that leaking from the package.

Before the next cycle can begin, the ballast volumes and associated lines must be pumped. Pumpdown time is determined by ballast volume, pumping speed, final pressures, and se-

quencing. Calculation indicates that a pump-down time of about 15 s is possible for ballast volumes of 10 ℓ and a mechanical pump rating of about 2.5 ℓ/s.

(S. Ruthberg and W. A. Cullins)

## 12.2. Calibration Stand for Gross Leaks

The hermetic test procedures in development (sec. 12.1) and interlaboratory comparisons such as those being conducted with tentative or draft procedures [56,57] in cooperation with ASTM Committee F-1 on Electronics (NBS Spec. Publs. 400-4, p. 67; 400-8, p. 40; and 400-12, pp. 33-34) require correlation of data to directly measured leaks. A general purpose vacuum system has been designed using available components and is being constructed to provide a facility for the measurement and calibration of gross leaks and vacuum gauges used in such test procedures. The vacuum circuit is shown schematically in figure 36; standard symbols [55] are used to indicate the components. Appropriate manifolds may be substituted for the test chamber to permit such procedures as leak measurement by rate-of-rise [58] and precision pressure point generation with reference to micromanometers for gauge calibration [59-61]. (S. Ruthberg and W. A. Cullins)

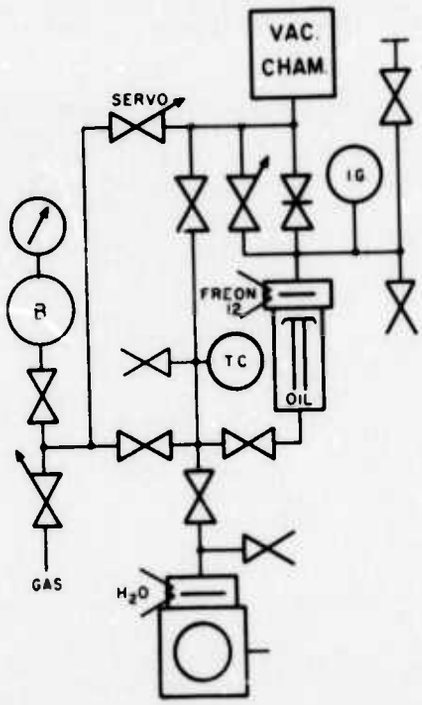



Figure 36. Vacuum circuit for calibration system for gross leaks and vacuum gauges.

# 13. THERMAL PROPERTIES OF DEVICES

## 13.1. Thermal Resistance Methods — Darlington Pairs

In a continuing effort to assess the feasibility of using electrical measurements to determine accurately some of the thermal properties of integrated Darlington transistors, measurements were made to verify several of the conclusions previously reached (NBS Spec. Pubis. 400-8, pp. 46-49, and 400-12, pp. 35-37).

Although most integrated Darlingtons are three-terminal devices for which some junction voltages cannot be measured independently, some Darlingtons have four terminals as depicted in figure 37. Since the four terminals are available for measurement, the individual emitter-base voltages of both the input and output transistors ($V_1$ and $V_2$, respectively) can be measured directly when the emitter-only switching method [62] is used. Measurements were made on a device of this type to test the validity of the assumptions made in deriving an expression for the thermal resistance of the output transistor, $R_{\theta JC2}$, (NBS Spec. Publ. 400-12, p. 37, eq (8))

$$R_{\theta JC2} = 2R_{\theta JC(1+2)} - R_{\theta JC1} \qquad (17)$$

where $R_{\theta JC(1+2)}$ is the thermal resistance determined by measuring the series combination of both emitter-base junctions (using the voltage $V_{12}$ as the temperature sensitive parameter) and $R_{\theta JC1}$ is the thermal resistance of the input transistor. In a three-terminal device, $R_{\theta JC2}$ cannot be measured independently. The assumptions made in deriving eq (17) are that the calibration constants for the input and output transistors are equal and that $R_{\theta JC1}$ can be measured with sufficient accuracy.

Most three-terminal Darlingtons contain integral bias resistors. To facilitate comparison with such devices, two resistors were added externally to the four-terminal Darlington as shown in figure 37. This is necessary because in the measurement of thermal resistance the presence of bias resistors necessitates a larger measuring current, $I_m$, than would be needed for an isolated discrete transistor in order to insure that the junction voltages used as temperature sensitive parameters vary relatively linearly with temperature.

The calibration constants of the individual transistors of the four terminal Darlington were determined for measuring currents of 7 and 50 mA. The results are listed in table 15. It can be seen that for $I_m$ = 50 mA they are essentially equal, whereas for $I_m$ = 7 mA there is a significant difference in their values. Thus, the assumption that the input and output transistors in an integrated Darlington pair have equal calibration constants appears to be reasonable if large values of $I_m$ are used.

A series of thermal resistance measurements was made on the four-terminal Darlington under various conditions. The results are summarized in table 16.

The thermal resistance, $R_{\theta JC1}$, of the input transistor, $Q_1$, was measured in three ways. First, the voltage $V_1$ was used as the temperature sensitive parameter (TSP) with $I_m$ = 7 or 50 mA and emitter-only switching [62]. This measurement is identical to that which would be performed on a discrete transistor if the emitter-base voltage were used as the TSP. Next, the voltage $V_{12}$ was used as the TSP, with emitter-only switching and a measuring current chosen large enough to turn $Q_1$ on but small enough to keep $Q_2$, the output transistor, off. The appropriate value depends on the magnitudes of $R_1$ and $R_2$ and their ratio; in the present case $I_m$ = 1 mA. Finally the collector-base voltage, $V_{CB1}$, was used as the TSP with $I_m$ = 1 mA and emitter-and-collector switching (NBS Tech. Note 743, pp. 34-35). This is sometimes necessary because the ratio or magnitudes of $R_1$ and $R_2$ may be such as to preclude a suitable measure of $R_{\theta JC1}$ from $V_{12}$ using a small value of $I_m$. The collector-base junction voltage is accessible on both three-terminal and four-terminal Darlingtons (NBS Spec. Publ. 400-12, p. 36). All three methods yielded essentially the same result for $R_{\theta JC1}$.

The thermal resistance, $R_{\theta JC2}$, of the output transistor, $Q_2$, was measured directly by using the voltage $V_2$ as the TSP with $I_m$ = 7 and 50 mA and emitter-only switching. Direct measurements of $R_{\theta JC2}$ using the collector-base junction of $Q_2$ as the temperature sensitive parameter proved unreliable

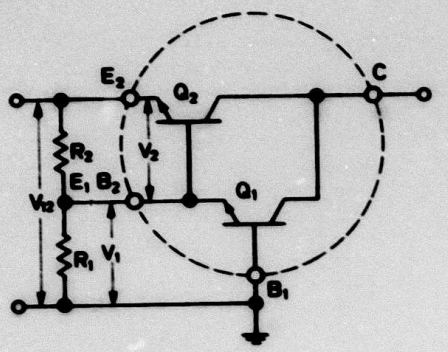



Figure 37. Four-terminal Darlington transistor with external resistors. ($R_1$ = 100 Ω; $R_2$ = 2200 Ω.)

Table 15 — Calibration Constants for a Four-Terminal Darlington Pair

| Transistor | $I_m$, mA | Constant, mV/°C |
|---|---|---|
| Input | 7 | 2.148 |
| Output | 7 | 1.883 |
| Input | 50 | 2.129 |
| Output | 50 | 2.029 |

Table 16 — Thermal Resistance Measurements on Four-Terminal Darlington

| Temperature Sensitive Parameter | Switching Method | $I_m$, mA | Quantity Determined | $R_{\theta JC}$, °C/W |
|---|---|---|---|---|
| $V_1$ | emitter-only | 7 | $R_{\theta JC1}$ | 3.00 |
| $V_1$ | emitter-only | 50 | $R_{\theta JC1}$ | 3.00 |
| $V_{12}$ | emitter-only | 1 | $R_{\theta JC1}$[a] | 2.96 |
| $V_{CB1}$ | emitter-and-collector | 1 | $R_{\theta JC1}$ | 2.92 |
| $V_2$ | emitter-only | 7 | $R_{\theta JC2}$ | 5.12 |
| $V_2$ | emitter-only | 50 | $R_{\theta JC2}$ | 4.84 |
| $V_{12}$ | emitter-only | 7 | $R_{\theta JC(1+2)}$ | 3.90 |
| $V_{12}$ | emitter-only | 50 | $R_{\theta JC(1+2)}$ | 3.84 |
| Computed from eq (17) | | 7[b] | $R_{\theta JC2}$ | 4.84 |
| Computed from eq (17) | | 50[b] | $R_{\theta JC2}$ | 4.72 |

[a] Value of $P_{\theta JC1}$ used in computation.

[b] Value of $I_m$ used for measuring $P_{\theta JC(1+2)}$.

Table 17 — Thermal Resistance Measurements on Integrated Darlington Transistors

| Device | $R_{\theta JC}$, °C/W | $I_C$, A | $V_{CE}$, V | $R_{\theta JC1}$, °C/W | $R_{\theta JC(1+2)}$, °C/W | $R_{\theta JC2}$, °C/W (Computed) | $R_{\theta JC2}$, °C/W (IR) |
|---|---|---|---|---|---|---|---|
| $T_2$[a] | 1.5 | 0.25 | 80 | 0.70 | 5.5 | 10.30 | 12.7 |
| $T_2$[a] | 1.5 | 0.25 | 76.5 | 0.61 | 4.05 | 7.49 | 10.7 |
| $T_2$ | 1.5 | 1.0 | 20 | 0.61 | 1.09 | 1.57 | 1.80 |
| 6M-1[b] | 1.75 | 3.5 | 20 | 0.59 | 1.13 | 1.67 | 2.19 |
| N-25[b] | 1.75 | 3.5 | 20 | 0.60 | 1.10 | 1.60 | 1.80 |

[a] These operating conditions caused a severe current constriction.

[b] Devices 6M-1 and N-25 bear same "2N" number but differ significantly in construction.

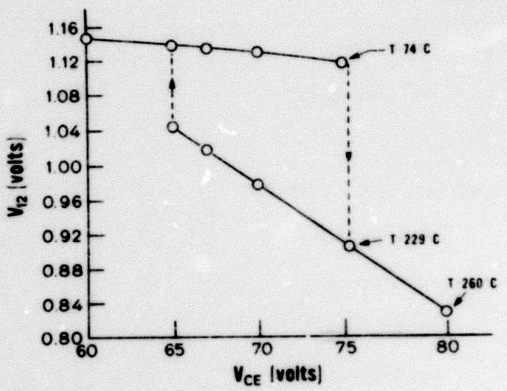



Figure 38. Voltage between output emitter and input base as a function of the collector-emitter voltage of the output transistor for a constant collector current showing onset of hot spot formation and thermal hysteresis. ($I_C$ = 0.25 A.)

because they varied greatly with the magnitude of $I_m$. The results of these measurements are therefore not included in the table.

Measurements of $V_{12}$ at relatively large values of $I_m$ using emitter-only switching result in values of thermal resistance, $R_{\theta JC(1+2)}$, intermediate between $R_{\theta JC1}$ and $R_{\theta JC2}$. While these values of thermal resistance are significantly lower than the directly measured value of $R_{\theta JC2}$, they can be combined with $R_{\theta JC1}$ (measured using $V_{12}$ and $I_m$ = 1 mA) according to eq (17) to compute $R_{\theta JC2}$. The calculated values are also listed in table 16 where it can be seen that they are 5.5 and 2.5 percent below the values measured directly with $I_m$ = 7 and 50 mA, respectively.

Measurements were made on several other devices to further test the validity of eq (17). The results of these measurements, all made on three terminal devices, are listed in table 17. Listed are the value specified by the manufacturer for the thermal resistance, $R_{\theta JC}$; operating conditions; $R_{\theta JC1}$ measured using a low value of measuring current; $R_{\theta JC(1+2)}$ measured using a high value of measuring current; $R_{\theta JC2}$ computed from eq (17); and $R_{\theta JC2}$ measured by means of an infrared microradiometer. The agreement between the computed $R_{\theta JC2}$ and the infrared measured $R_{\theta JC2}$ is not significantly different than might be expected for measurements on discrete devices even in the cases where a severe current constriction occurs.

As noted in table 17, the output transistor of device $T_2$ had a severe current constriction for two of the operating conditions listed. It was found that the input-base current changed only from 4.00 to 4.06 mA when the constriction formed. Thus, in contrast to the case for a discrete transistor [63] the dc current gain does not provide a satisfactory indicator of the formation of current constrictions in Darlingtons. This is because of the small magnitude of the input base current, particularly for the high voltage-low current case where severe current constriction and thermal hysteresis occur, and also because of the bypass effect of the bias resistors. However, the voltage $V_{12}$ between the input-base and output-emitter measured during the power-off portion of the emitter-only switching method of the thermal resistance measuring cycle was found to be an excellent substitute. This is illustrated for device $T_2$ in figure 38 which shows $V_{12}$ as a function of collector-emitter voltage, $V_{CE}$, for a collector current, $I_C$, of 0.25 A as the current constriction forms and the device goes through thermal hysteresis. (S. Rubin)

## 13.2. Transient Thermal Response

Work continued on the development of a measurement technique based upon electrical measurements for estimating the peak junction temperature of power transistors. This technique requires that the total available active area of the device, $A_T$, be known because it is assumed that the low level sampling current, $I_m$, is uniformly distributed throughout $A_T$ during calibration, but that $I_m$ is confined to the area of power generation, $A_E$, during measurement. As discussed previously (NBS Spec. Publ. 400-12, pp. 37-40), if $A_T$ is known, the calibration curve can be corrected to account for the increased sampling current density during measurement.

Measurements made on numerous devices showed that the heating response of a device can be used to estimate $A_T$ satisfactorily. If it is assumed that the current is uniformly distributed throughout $A_T$ during the heating pulse, that the heat flow is one dimensional, and that the principle of superposition can be applied, the total available active area of the device is given by

$$A_T = \frac{2P}{\sqrt{\rho k c \pi}} \frac{[\sqrt{t_1 + t_2} - \sqrt{t_2}]}{[T(t_2) - T(0)]}, \qquad (18)$$

where P is the power applied during the pulse in watts, $\rho$ is the mass density in gram per cubic centimetre, k is the thermal conductivity in watts per centimeter kelvin, c is the thermal capacity in watt seconds per gram kelvin, $t_1$ is the width of the heating pulse in seconds, $t_2$ is the time

between the end of the heating pulse and the measurement in seconds, $T(t_2)$ is the junction temperature at the time of measurement in degrees Celsius, and $T(0)$ is the junction temperature before power is applied in degrees Celsius. The power applied must be great enough to raise the junction temperature by at least 30°C to achieve adequate measurement precision. The pulse width was chosen as 1 ms because this pulse width is generally long enough to result in a satisfactory temperature rise for reasonable power levels while it is not too long to invalidate the assumption of uniform current distribution. This is most likely to be the situation for current levels near but below the maximum allowed current, $I_{C(max)}$, for the device. Measurements were made on a number of devices with the result that the value of $A_T$ calculated from eq (18) usually varied by less than 10 percent when the heating current varied from $\frac{1}{2}I_{C(max)}$ to $I_{C(max)}$. Eq (18) contains a correction to allow for cooling during the delay following the end of the heating pulse. This delay is necessary to allow electrical switching transients to subside before a reliable electrical measurement can be made.

The computer model used to simulate the temperature distribution on the surface of a silicon chip heated in a central region was refined by the inclusion of a copper slug between the chip and the heat sink. The results of Kokkas [64] were used for this refinement which enables the model to simulate better an actual device. Curves of the electrically measured average junction temperature expressed as a fraction of the peak junction temperature are plotted against the effective size of the heat source at steady state in figure 39. The three curves are for chips 100 mil (2.5 mm), 150 mil (3.8 mm) and 200 mil (5.1 mm) on a side. The silicon chip was chosen to be 10 mil (0.25 mm) thick. These curves are for the silicon chip resting on a copper slug, 50 mil (1.3 mm) thick, which in turn rests on an infinite heat sink. It is interesting to note that the inclusion of the copper slug has an insignificant effect on the curve for the 100 mil chip previously reported (NBS Spec. Publ. 400-12, pp. 39-40). However, the curves for the 150 mil and 200 mil chips do show differences between the two models. (D. L. Blackburn)

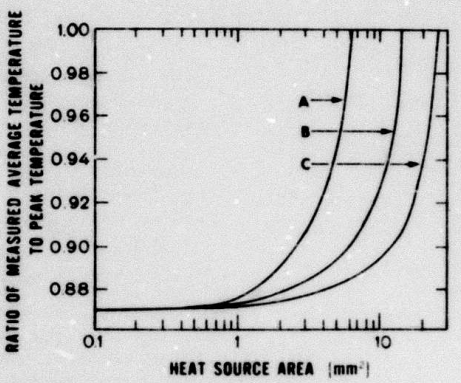



Figure 39. Electrically measured average junction temperature as a function of the area of heat source. (Curve A: side of chip, 100 mil (2.5 mm); Curve B: side of chip, 150 mil (3.8 mm); Curve C: side of chip, 200 mil (5.1 mm).)

# 14. REFERENCES


1. Rupprecht, D., and Stach, J., Oxidized Boron Nitride Wafers as an *In-Situ* Boron Dopant for Silicon Diffusions, *J. Electrochem. Soc.* 120, 1266-1271 (1973).

2. Kriegler, R. J., The Uses of HCl and $Cl_2$ for the Preparation of Electrically Stable $SiO_2$, *Semiconductor Silicon/1973*, H. R. Huff and R. R. Burgess, eds., pp. 363-375 (Electrochemical Society, Princeton, New Jersey, 1974.

3. Buehler, M. G., *Semiconductor Measurement Technology:* Microelectronic Test Patterns: An Overview, NBS Spec. Publ. 400-6 (August 1974).

4. Buehler, M. G., Thermally Stimulated Measurements: The Characterization of Defects in Silicon *p-n* Junctions, *Semiconductor Silicon/1973*, H. R. Huff and R. R. Burgess, eds., pp. 549-560 (Electrochemical Society, Princeton, New Jersey, 1974).

5. Hofstein, S. R., Minority Carrier Lifetime Determination from Inversion Layer Transient Response, *IEEE Trans. Electron Devices* ED-14, 785-786 (1967).

6. Silicon Resistivity Standards, SRM-1520, Office of Standard Reference Materials, National Bureau of Standards, Washington, D. C. 20234.

7. Standard Method for Measuring Resistivity of Silicon Slices with a Collinear Four-Probe Array, ASTM Designation F 84, *Annual Book of ASTM Standards*, Part 43 (November 1974). (Available as a separate reprint from American Society for Testing and Materials, 1916 Race Street, Philadelphia, Pa. 19103.)

8. Grove, A. S., *Physics and Technology of Semiconductor Devices*, p. 272 (John Wiley and Sons, Inc., New York, 1967).

9. Kraft, R., Finite Difference Techniques for Diffusion and Redistribution Problems with Segregation-type Boundary Conditions, *Proceedings of the AICA International Symposium on Computer Methods for Partial Differential Equations*, Lehigh University, Bethlehem, Pa., June 17-19, 1975, pp. 328-334.

10. Isaacson, E., and Keller, H. B., *Analysis of Numerical Methods*, pp. 55-58 (John Wiley and Sons, Inc., New York, 1966).

11. Grove, A., Leistiko, Jr., O., and Sah, C. T., Redistribution of Acceptor and Donor Impurities during Thermal Oxidation of Silicon, *J. Appl. Phys.* 35, 2695-2701 (1964).

12. Irvin, J. C., Resistivity of Bulk Silicon and of Diffused Layers in Silicon, *Bell System Tech. J.* 41, 387-410 (1962).

13. Bullis, W. M., Brewer, F. H., Kolstad, C. D., and Swartzendruber, L. J., Temperature Coefficient of Resistivity of Silicon and Germanium near Room Temperature, *Solid-State Electronics* 11, 639-646 (1968).

14. Caughey, D. M., and Thomas, R. E., Carrier Mobilities in Silicon Empirically Related to Doping and Field, *Proc. IEEE* 55, 2192-2193 (1967).

15. Aubuchon, K. G., Radiation-Hardened MOSFETS, Final Technical Report, Contract N00014-71-C-0079 (Huges Research Laboratories, Malibu, California, March 1972).

16. Dick, C. E., Lucas, A. C., Motz, J. W., Placious, R. C., and Sparrow, J. H., Large-Angle X X-ray Production by Electrons, *J. Appl. Phys.* 44, 815-826 (1973).

17. Veigele, W. J., Photon Cross Sections from 0.1 keV to 1 MeV for Elements Z = 1 to Z = 99, *Atomic Data Tables* 5, 51-111 (1973).

18. Standard Method of Test for Thickness of Epitaxial or Diffused Layers in Silicon by the Angle Lapping and Staining Technique, ASTM Designation F 110, *Annual Book of ASTM Standards*, Part 43 (November 1974). (Available as a separate reprint from American Society for Testing and Materials, 1916 Race Street, Philadelphia, Pennsylvania 19103.)

19. Standard Method for Measuring Hall Mobility and Hall Coefficient in Extrinsic Semiconductor Single Crystals, ASTM Designation F 76, *Annual Book of ASTM Standards*, Part 43 (November 1974). (Available as a separate reprint from American Society for Testing and Materials, 1916 Race Street, Philadelphia,

Pennsylvania 19103.)

20. van der Pauw, L. S., A Method of Measuring the Resistivity and Hall Coefficients on Lamella of Arbitrary Shape, *Philips Research Reports* 13, 1-9 (1958).

21. Penney, W. M., and Lau, L., Eds., *MOS Integrated Circuits*, pp. 113-116 (van Nostrand, Reinhold Company, New York, 1972).

22. Uhlir, A., Jr., The Potentials of Infinite Systems of Sources and Numerical Solutions of Problems in Semiconductor Engineering, *Bell System Tech. J.* 34, 105-128 (1955).

23. Swartzendruber, L. J., Correction Factor Tables for Four-Point Probe Resistivity Measurements on Thin Circular Semiconductor Samples, NBS Tech. Note 199 (April 15, 1964) (Available from National Technical Information Service, Springfield, Virginia 22161, Accession No. AD 683 408).

24. Mattis, R. L., and Buehler, M. G., *Semiconductor Measurement Technology:* A BASIC Program for Calculating Dopant Density Profiles from Capacitance-Voltage Data, NBS Spec. Publ. 400-11 (June 1975).

25. Sittig, E. K., Feldman, M., Townsend, R. L., and Kinsel, T. S., An Automated Inspection System for Integrated Circuit Masks with Replicated Patterns, Micro-Electronics Seminar, Interface '73, Atlanta, Georgia, October 29-30, 1973. (Available from Eastman Kodak Co., 343 State Street, Dept. 454, Rochester, N. Y. 14650, Kodak Publication No. G-35.)

26. Ciarlo, D. R., Schultz, P. A., and Novotny, D. B., Automated Inspection of IC Photomasks, *Proc. Soc. Photo-Optical Instrumentation Engineers*, Vol. 55, Technological Advances in Micro and Submicro Photofabrication Imagery, San Diego, California, August 21-23, 1974, pp. 84-89.

27. Dyer, D. L., Optical Limits in TV Microscopy, *Research/Development* 24, 40-44 (September 1973).

28. Hyzer, William G., Image Analysis, *Research/Development* 25, 44-49 (February 1974).

29. Kossyk, G. J. W., Laico, J. P., Rongvd, L., and Stafford, J. W., The Primary Pattern Generator Part II — Mechanical Design, *Bell Syst. Tech. J.* 49, 2043-2059 (1970).

30. Chitayat, Anwar K., High Speed Positioning, *Solid State Technology* 16, 42-44 (June 1973).

31. Hartman, D. K., Glasbrenner, F. K., and Colangelo, D., Part I Manufacturing In-Process Control and Measuring Techniques of Mask Evaluations, AFML-TR-69-334 Technical Report, December 1970. (Available to qualified requestors from the Defense Documentation Center, Cameron Station, Alexandria, Virginia 22314, Accession No. AD 881208.)

32. Bourdelais, R. J., Colangelo, D., McFadyen, R. J., and Elliott, J. F., Instrument for Automatically Inspection Integrated Circuit Masks for Pinholes and Spots, U.S. Patent 3,795,452, March 5, 1974. (Government-owned invention available for licensing; copy of patent available from Commissioner of Patents, Washington, D. C. 20231.)

33. Cook, H. D., and Marzetta, L. A., An Automatic Fringe Counting Interferometer for use in the Calibration of Line Scales, *J. Res. Natl. Bur. Stand. (U.S.)* 65C, 129-139 (1961).

34. Gentry, F. E., Gutzwiller, F. W., Holonyak, Jr., N., and Von Zastrow, E. E., *Semiconductor Controlled Rectifiers*, pp. 42-52 (Prentice-Hall, Inc., Englewood Cliffs, New Jersey, 1964).

35. Grove, A. S., *Physics and Technology of Semiconductor Devices*, pp. 264-271 (John Wiley and Sons, Inc., New York, 1967).

36. Buehler, M. G., Impurity Centers in *p-n* Junctions Determined from Shifts in the Thermally Stimulated Current and Capacitance Response with Heating Rate, *Solid-State Electronics* 15, 69-79 (1972).

37. Goetzberger, A., and Nicollian, E. H., MOS Avalanche and Tunneling Effects in Silicon Surfaces, *J. Appl. Phys.* 38, 4582-4588 (1967).

38. Green, D., Sandor, J. E., O'Keeffe, T. W., and Matta, R. K., Reversible Changes in Transistor Characteristics Caused by Scanning Electron Microscope Examination, *Appl. Phys. Letters* 6, 3-4 (1965).

39. Thornton, P. R., Hughes, K. A., Kyaw, H., Millward, C., and Sulway, D. V., Failure Analysis of Microcircuitry by Scanning Electron Microscopy, *Microelectronics and Reliability* 6, 9-16 (1967).

40. Lipman, J. A., Bruncke, W. C., Crosthwait, D. L., Galloway, K. F., and Pease, R. L., Use of a Scanning Electron Microscope for Screening Bipolar Surface Effects, *IEEE Trans. Nucl. Sci.* NS-21, No. 6, 383-386 (1974).

41. Pease, R. L., and Galloway, K. F., Degradation of Bipolar Transistor Electrical Parameters During SEM Evaluation, *Microelectronics and Reliability* 13, 549-550 (1974).

42. Snow, E. H., Grove, A. S., and Fitzgerald, D. J., Effects of Ionizing Radiation on Oxidized Silicon Surfaces and Planar Devices, *Proc. IEEE* 55, 1168-1185 (1967).

43. Szedon, J. R., and Sandor, J. E., The Effect of Low-Energy Electron Irradiation of Metal-Oxide-Semiconductor Structures, *Appl. Phys. Letters* 6, 181-182 (1965).

44. Speth, A. J., and Fang, F. F., Effects of Low-Energy Electron Irradiation on Si-Insulated Gate FETs, *Appl. Phys. Letters* 7, 145-146 (1965).

45. Simons, M., Monteith, K. L., and Hauser, J. R., Some Observations on Charge Buildup and Release in Silicon Dioxide Irradiated with Low Energy Electrons, *IEEE Trans. Electron Devices* ED-15, 966-973 (1968).

46. MacDonald, N. C., and Everhart, T. E., Selective Electron-Beam Irradiation of Metal-Oxide-Semiconductor Structures, *J. Appl. Phys.* 39, 2433-2447 (1968).

47. MacDonald, N. C., Quantitative Scanning Electron Microscopy: Solid State Applications, *Scanning Electron Microscopy/1969*, O. Johari and I. Corvin, eds., pp. 431-437 (IITRI, Chicago, Illinois, 1969).

48. Thomas, A. G., Butler, S. R., Goldstein, J. I., and Parry, P. D., Electron Beam Irradiation Effects in Thick-Oxide MOS Capacitors, *IEEE Trans. Nucl. Sci.* NS-21, No. 4, 14-19 (1974).

49. Cohen, S., and Hughes, H., SEM Irradiation for Hardness Assurance Screening and Process Definition, *IEEE Trans. Nucl. Sci.* NS-21, No. 6, 387-389 (1974).

50. Everhart, T. E., and Hoff, P. H., Determination of Kilovolt Electron Energy Dissipation vs. Penetration Distance in Solid Materials, *J. Appl. Phys.* 42, 5837-5846 (1971).

51. Bishop, H. E., Electron Scattering in Thick Targets, *Brit. J. Appl. Phys.* 18, 703-715 (1967).

52. Pugh, J. W., The Temperature Dependence of Preferred Orientation in Rolled Tungsten, *Trans. AIME* 212, 637-642 (1958).

53. Swalin, R. A., and Geisler, A. H., The Recrystallization Process in Tungsten as Influenced by Impurities, *J. Inst. Metals* 86, 129-134 (1957).

54. Robinson, Dr., C. S., Rate of Crystal Growth in Drawn Tungsten Wire as a Function of Temperature, *J. Appl. Phys.* 13, 647-651 (1942).

55. Graphic Symbols in Vacuum Technology, Am. Vac. Soc. Standard 7.1-1966, *J. Vac. Sci. Technol.* 4, 139-142 (1967).

56. Tentative Recommended Practices for Determining Hermeticity of Electron Devices with a Helium Mass Spectrometer Leak Detector, ASTM Designation F 134, *Annual Book of ASTM Standards*, Part 43 (November 1974). (Available as a separate reprint from American Society for Testing and Materials, 1916 Race Street, Philadelphia, Pennsylvania, 19103.)

57. Draft Recommended Practices for Determining Hermeticity of Electron Devices by a Radioisotope Test, ASTM Committee F-1 Draft 8005 (unpublished).

58. Method for Vacuum Leak Calibration, Am. Vac. Soc. Standard 2.2-1968, *J.*

*Vac. Sci. Technol.* 5, 219-222 (1968).

59. Ruthberg, S., Calibration to High Precision in the Medium Vacuum Range with Stable Environments and Micromanometer, *J. Vac. Sci. Technol.* 6, 401-412 (1969).

60. Procedure for Calibrating Vacuum Gauges of the Thermal Conductivity Type, Am. Vac. Soc. Standard 6.2-1969, *J. Vac. Sci. Technol.* 6, 977-980 (1969).

61. Procedure for Calibrating Hot Filament Ionization Gauges Against a Reference Manometer in the Range $10^{-2}$ to $10^{-5}$ Torr, Am. Vac. Soc. Standard 6.4-1969, *J. Vac. Sci. Technol.* 7, 370-374 1970).

62. Thermal Resistance Measurements of Conduction Cooled Power Transistors, JEDEC Publication No. 91, August 1974. (Available from Engineering Department, Electronic Industries Association, 2001 Eye Street, N.W., Washington, D. C. 20006.)

63. Oettinger, F. F., and Rubin, S., The Use of Current Gain as an Indicator for the Formation of Hot Spots Due to Current Crowding in Power Transistors, *Tenth Annual Proceedings, Reliability Physics 1972*, Las Vegas, Nevada, pp. 12-18. (Available from Publication Sales Dept., The IEEE, 345 E. 47th Street, New York, New York 10017, Catalog No. 72CH0628-8-PHY).

64. Kokkas, A. G., Thermal Analysis of Multiple-Layer Structures, *IEEE Trans. Electron Devices* ED-21, 674-681 (1974).

APPENDIX A

# SEMICONDUCTOR TECHNOLOGY PROGRAM STAFF

Coordinator: J. C. French*
Secretary: Miss B. S. Hope*
Consultant: C. P. Marsden‡

## Semiconductor Characterization Section

(301) 921-3625

Dr. W. M. Bullis, Chief
Dr. M. G. Buehler, Asst. Chief

F. H. Brewer
Miss F. C. Butler+
M. Cosman
Mrs. K. E. Dodson+
Dr. J. R. Ehrstein
Dr. R. Y. Koyama
Dr. A. G. Lieberman
R. L. Mattis
Dr. S. Mayo
Dr. W. E. Phillips
Miss D. R. Ricks
L. M. Smith
Mrs. M. L. Stream+
W. R. Thurber

## Semiconductor Processing Section

(301) 921-3541

Dr. A. H. Sher, Chief
S. Ruthberg, Asst. Chief — Assembly
H. A. Schafft, Asst. Chief — Processing

Dr. J. H. Albers
Mrs. C. A. Cannon
W. A. Cullins
G. G. Harman
Miss D. L. Hines+
H. K. Kessler
J. Kr wczyk
T. F. Leedy
Y. M. Liu
Dr. D. B. Novotny
R. L. Raybold
I. Szabo
Mrs. E. Y. Trager

## Electron Devices Section

(301) 921-3622

F. F. Oettinger, Acting Chief

D. W. Berning
D. L. Blackburn
H. E. Dyson
Dr. K. F. Galloway
Mrs. A. D. Glover+
W. J. Keery
Mrs. K. O. Leedy
Dr. D. C. Lewis
Mrs. B. A. Oravec¶+
M. K. Phillips
G. J. Rogers
S. Rubin
D. E. Sawyer
M. W. Stoops¶
L. R. Williams

---

¶ Part Time
\+ Secretary
* Telephone: (301) 921-3357
‡ Telephone: (301) 921-3621

## APPENDIX B

# SEMICONDUCTOR TECHNOLOGY PROGRAM PUBLICATIONS

### B.1. Prior Reports

A review of the early work leading to this Program is given in Bullis, W. M., Measurement Methods for the Semiconductor Device Industry — A Review of NBS Activity, NBS Tech. Note 511 (December 1969).

Progress reports covering the period July 1, 1968, through June 30, 1973, were published as NBS Technical Notes with the title, Methods of Measurement for Semiconductor Materials, Process Control, and Devices:

| Quarter Ending | NBS Tech. Note | Date Issued | NTIS Accession No. |
|---|---|---|---|
| eptember 30, 1968 | 472 | December 1968 | AD 681330 |
| December 31, 1968 | 475 | February 1969 | AD 683808 |
| March 31, 1969 | 488 | July 1969 | AD 692232 |
| June 30, 1969 | 495 | September 1969 | AD 695820 |
| September 30, 1969 | 520 | March 1970 | AD 702833 |
| December 31, 1969 | 527 | May 1970 | AD 710906 |
| March 31, 1970 | 555 | September 1970 | AD 718534 |
| June 30, 1970 | 560 | November 1970 | AD 719976 |
| September 30, 1970 | 571 | April 1971 | AD 723671 |
| December 31, 1970 | 592 | August 1971 | AD 728611 |
| March 31, 1971 | 598 | October 1971 | AD 732553 |
| June 30, 1971 | 702 | November 1971 | AD 734427 |
| September 30, 1971 | 717 | April 1972 | AD 740674 |
| December 31, 1971 | 727 | June 1972 | AD 744946 |
| March 31, 1972 | 733 | September 1972 | AD 748640 |
| June 30, 1972 | 743 | December 1972 | AD 753642 |
| September 30, 1972 | 754 | March 1973 | AD 757244 |
| December 31, 1972 | 773 | May 1973 | AD 762840 |
| March 31, 1973 | 788 | August 1973 | AD 766918 |
| June 30, 1973 | 806 | November 1973 | AD 771018 |

After July 1, 1973, progress reports were issued in the NBS Special Publication 400 subseries with the title, Semiconductor Measurement Technology:

| Quarter Ending | NBS Spec. Publ. | Date Issued | NTIS Accession No. |
|---|---|---|---|
| September 30, 1973 | 400-1 | March 1974 | AD 775919 |
| December 31, 1973<br>March 31, 1974 | 400-4 | November 1974 | COM 74-51222 |
| June 30, 1974 | 400-8 | February 1975 | AD/A 005669 |
| September 30, 1974 | 400-12 | May 1975 | AD/A 011121 |

### B.2. Current Publications

As various phases of the work are completed, publications are prepared to summarize the results or to describe the work in greater detail. Publications of this kind which have been issued recently are listed below:

Ciarlo, D. R., Schultz, P. A., and Novotny, D. B., Automated Inspection of IC Photomasks, *Proc. Soc. Photo-Optical Instrumentation Engineers*, Vol. 55, Technological Advances in Micro and Sub-Micro Photofabrication Imagery, Society of Photo-Optical Instrumentation Engineers, San Diego, California, August 21-23, 1974, pp. 84-89.

Marsden, C. P., Tabulation of Published Data on Electron Devices in the U.S.S.R. Through December 1973, NBS Technical Note 835 (November 1974). (Supersedes NBS Technical Note 715.)

**Ehrstein, J. R., Ed.,** *Semiconductor Measurement Technology:* **Spreading Resistance Symposium, NBS Spec. Publ. 400-10 (December 1974).**

**Schafft, H. A.,** *Semiconductor Measurement Technology:* **ARPA/NBS Workshop II. Hermeticity Testing for Integrated Circuits, NBS Spec. Publ. 400-9 (December 1974).**

**Ehrstein, J. R., Improved Surface Preparation for Spreading Resistance Measurements on** *p*-**Type Silicon,** *Semiconductor Measurement Technology:* **Spreading Resistance Symposium, J. R. Ehrstein, Ed., NBS Spec. Publ. 400-10 (December 1974), pp. 249-255.**

**Rogers, G. J., Sawyer, D. E., and Jesch, R. L.,** *Semiconductor Measurement Technology:* **Measurement of Transistor Scattering Parameters, NBS Spec. Publ. 400-5 (January 1975).**

**Sher, A. H.,** *Semiconductor Measurement Technology:* **Improved Infrared Response Technique for Detecting Defects and Impurities in Germanium and Silicon** *p-i-n* **Diodes, NBS Spec. Publ. 400-13 (February 1975).**

**Lewis, D. C., On the Determination of the Minority Carrier Lifetime from the Reverse Recovery Transient of** *pnN* **Diodes,** *Solid-State Electronics* **18, 87-91 (January 1975).**

**Blackburn, D. L., An Electrical Technique for the Measurement of the Peak Junction Temperature of Power Transistors,** *Thirteenth Annual Proceedings, Reliability Physics 1975,* **Las Vegas, Nevada, April 1-3, 1975, to appear.**

**Blackburn, D. L., and Oettinger, F. F., Transient Thermal Response of Measurements of Power Transistors,** *IEEE Trans. Industrial Electronics and Control Instrumentation* **IECI-22, 134-141 (May 1975).**

**Galloway, K. F., Keery, W. J., and Leedy, K. O., Integrated Circuit Damage Resulting from SEM Examination,** *Proc. 25th Annual Electronic Components Conference,* **Washington, D. C., May 12-14, 1975, pp. 263-266.**

**Buehler, M. G., Planar Test Structures for Characterizing Impurities in Silicon,** *Extended Abstracts* **of the Meeting of the Electrochemical Society, Toronto, Ontario, May 11-16, 1975, pp. 403-404.**

**Rubin, S., Thermal Resistance Measurements on Monolithic and Hybrid Darlington Power Transistors,** *Proceedings 1975 IEEE Power Electronics Specialists Conference (PESC),* **Culver City, California, June 9-11, 1975, to appear.**

**Kraft, R., Finite Difference Techniques for Diffusion and Redistribution Problems with Segregation-type Boundary Conditions,** *Proceedings of the AICA International Symposium on Computer Methods for Partial Differential Equations,* **Lehigh University, Bethlehem, Pa., June 17-19, 1975, pp. 328-334.**

## B.3. Availability of Publications

**In most cases reprints of articles in technical journals may be obtained on request to the author. NBS Technical Notes and Special Publications are available from the Superintendent of Documents, U.S. Government Printing Office, Washington, D. C. 20402, or the National Technical Information Service, Springfield, Virginia 22161, or both. Current information regarding availability of all publications issued by the Program is provided in the latest edition of NBS List of Publications No. 72 which can be obtained on request to Mrs. K. O. Leedy, Room B346, Technology Building, National Bureau of Standards, Washington, D. C. 20234.**

## B.4. Videotapes

**Color videotape cassette presentation on improvements in semiconductor measurement**

technology are being prepared for the purpose of more effectively disseminating the results of the work to the semiconductor industry. These videotapes are available for distribution on loan without charge on request to H. A. Schafft, Room A317, Technology Building, National Bureau of Standards, Washington, D. C. 20234. Copies of these videotapes may be made and retained by requestors. The first videotape, Defects in PN Junctions and MOS Capacitors Observed Using Thermally Stimulated Current and Capacitance Measurements, by M. G. Buehler has been completed and released for distribution. As an added feature, arrangements can be made for the author to be available for a telephone conference call to answer questions and provide more detailed information, following a prearranged showing of the videotape.

APPENDIX C

# WORKSHOP AND SYMPOSIUM SCHEDULE

C.1. Proceedings or Reports of Past Events:

Symposium on Silicon Device Processing, Gaithersburg, Maryland, June 2-3, 1970. (Cosponsored by ASTM Committee F-1 and NBS). Proceedings: NBS Spec. Publ. 337 (November 1970).

ARPA/NBS Workshop I. Measurement Problems in Integrated Circuit Processing and Assembly, Palo Alto, California, September 7, 1973. Report: NBS Spec. Publ. 400-3 (January 1974).

ARPA/NBS Workshop II. Hermeticity Testing for Integrated Circuits, Gaithersburg, Maryland, March 29, 1974. Report: NBS Spec. Publ. 400-9 (December 1974).

Spreading Resistance Symposium, Gaithersburg, Maryland, June 13-14, 1974. (Cosponsored by ASTM Committee F-1 and NBS). Proceedings: NBS Spec. Publ. 400-10 (December 1974).

ARPA/NBS Workshop III. Test Patterns, Scottsdale, Arizona, September 6, 1974. Report: NBS Spec. Publ. 400-15 (to appear).

ARPA/NBS Workshop IV. Surface Analysis for Silicon Devices, Gaithersburg, Maryland, April 23-24, 1975. Report: NBS Spec. Publ. 400-23 (to appear)

C.2. Calendar of Future Events:

Reliability Technology for Cardiac Pacemakers, Gaithersburg, Maryland, July 28-29, 1975 (Workshop cosponsored by Food and Drug Administration and NBS).

## APPENDIX D

# STANDARDS COMMITTEE ACTIVITIES

ASTM Committee F-1 on Electronics

J. H. Albers, Secretary, Packaging Subcommittee; Hybrid Microelectronics Subcommittee

M. G. Buehler, Chairman, Task Force on Test Patterns, Process Controls Section; Semiconductor Crystals and Semiconductor Measurements Subcommittees

W. M. Bullis, Secretary; Editor, Semiconductor Crystals Subcommittee

J. R. Ehrstein, Chairman, Resistivity Section; Semiconductor Crystals and Semiconductor Measurements Subcommittees

J. C. French, Chairman, Editorial Subcommittee; Awards Committee

G. G. Harman, Secretary, Interconnection Bonding Section; Hybrid Microelectronics Subcommittee

K. O. Leedy, Chairman, Packaging Subcommittee; Chairman, Interconnection Bonding Section; Hybrid Microelectronics and Quality and Hardness Assurance Subcommittees

D. C. Lewis, Semiconductor Measurements and Quality and Hardness Assurance Subcommittees

C. P. Marsden, Honorary Chairman

R. L. Mattis, Editor, Semiconductor Measurements Subcommittee; Semiconductor Crystals Subcommittee

J. F. Mayo-Wells, Secretary, Editorial Subcommittee

D. B. Novotny, Editor, Semiconductor Processing Materials Subcommittee

W. E. Phillips, Chairman, Lifetime Section; Secretary, Semiconductor Crystals Subcommittee; Semiconductor Processing Materials, Semiconductor Measurements, and Hybrid Microelectronics Subcommittees

G. J. Rogers, Quality and Hardness Assurance Subcommittee

S. Ruthberg, Chairman, Hermeticity Section; Semiconductor Processing Materials, Hybrid Microelectronics, and Quality and Hardness Assurance Subcommittees

H. A. Schafft, Chairman, Publicity Committee

A. H. Sher, Semiconductor Crystals, Semiconductor Processing Materials, and Hybrid Microelectronics Subcommittees

W. R. Thurber, Semiconductor Crystals and Semiconductor Measurements Subcommittees

ASTM Committee E-10 on Radioisotopes and Radiation Effects

W. M. Bullis, Subcommittee 7, Radiation Effects on Electronic Materials

J. C. French, Subcommittee 7, Radiation Effects on Electronic Materials

D. C. Lewis, Subcommittee 7, Radiation Effects on Electronic Materials

Electronic Industries Association: Solid State Products Division, Joint Electron Device Engineering Council (JEDEC)

F. F. Oettinger, Chairman, Task Group JC-11.3-1 on Thermal Considerations for Microelectronic Devices, Committee JC-11.3 on Mechanical Standardization for Microelectronic Devices; Chairman, Task Group JC-25-5 on Thermal Characterization of Power Transistors, Committee JC-25 on Power Transistors; Technical Advisor, Thermal Properties of Devices, Committees JC-13.1 on Government Liaison for Discrete Semiconductor Devices, JC-22 on Rectifier Diodes and Thyristors, JC-20 on Signal and Regulator Diodes, and JC-30 on Hybrid Integrated Circuits

S. Rubin, Chairman, Council Task Group on Galvanomagnetic Devices

D. E. Sawyer, Task Group JC-24-5 on Transistor Scattering Parameter Measurement Standard, Committee JC-24 on Low Power Transistors

H. A. Schafft, Technical Advisor, Second Breakdown and Related Specifications Committee JC-25 on Power Transistors

Electronic Industries Association: Government Products Division

F. F. Oettinger, Chairman, Task Group G-12-08-74 on Recommendations for Military Usage of Proposed Standards and Test Methods for Thermal Resistance, Committee G-12 on Solid State Devices

IEEE Electron Devices Group

J. C. French, Standards Committee

F. F. Oettinger, Standards Committee Task Force on Second Breakdown Measurement Standards

H. A, Schafft, Standards Committee Task Force on Second Breakdown Measurement Standards

IEEE Magnetics Group

S. Rubin, Chairman, Galvanomagnetic Standards Subcommittee

Society of Automotive Engineers

J. C. French, Subcommittee A-2N on Radiation Hardness and Nuclear Survivability

W. M. Bullis, Planning Subcommittee of Committee H on Electronic Materials and Processes

IEC TC47, Semiconductor Devices and Integrated Circuits

S. Rubin, Technical Expert, Galvanomagnetic Devices; U.S. Specialist for Working Group 5 on Hall Devices and Magnetoresistive Devices

APPENDIX E

# SOLID-STATE TECHNOLOGY & FABRICATION SERVICES

Technical services in areas of competence are provided to other NBS activities and other government agencies as they are requested. Usually these are short-term, specialized services that cannot be obtained through normal commercial channels. Such services provided during the last quarter, which are listed below, indicate the kinds of technology available to the program.

E.1. Semiconductor Device Fabrication (J. Krawczyk and T. F. Leedy)

MOS capacitors with gates transparent to ultraviolet radiation were fabricated for the Harry Diamond Laboratories.

E.2. Scribing (J. Krawczyk)

Iron-oxide-coated glass substrates were cut to size using the wafer scriber for the Harry Diamond Laboratories.

E.3. Thermocouple Repair (H. K. Kessler)

Miniature multijunction thermocouples were repaired for the NBS Electricity Division.

E.4. Semiconductor Device Assembly (H. K. Kessler)

Silicon wafers containing fifty arrays were diced and mounted to TO-5 headers for the Army Electronics Command, Fort Monmouth, New Jersey. The interconnections were made by means of ultrasonic bonding using aluminum and silver ribbon wire. These devices are to be used for current density studies.

E.5. Scanning Electron Microscopy (W. J. Keery)

Scanning Electron Micrographs were taken of various cement samples for the NBS Materials and Composites Section.

Scanning electron micrographs were made of diesel exhaust smoke particles for the NBS Fire Technology Division.

A specimen of a Moire pattern test structure was examined for the NBS Optics and Micrometrology Section.

**Announcement of New Publications on Semiconductor Measurement Technology**

Superintendent of Documents,
Government Printing Office,
Washington, D.C. 20402

Dear Sir:

Please add my name to the announcement list of new publications to be issued in the series: National Bureau of Standards Special Publication 400–.

Name _____

Company _____

Address _____

City _____ State _____ Zip Code _____

(Notification Key N-413)

# INDEX

CALL FOR LEVEL OF INTEREST

# WORKSHOP ON MICRODEFECTS - THEIR CHARACTERIZATION AND EFFECTS ON SILICON DEVICES

SPONSOR: ASTM Committee F-1 on Electronics

WHEN: September 16, 1976, in conjunction with the meeting of Committee F-1, September 14-16, 1976

WHERE: Town and Country Hotel - San Diego, California

WHAT: A series of invited papers is planned covering the following areas:

- A general survey of the field of microdefects in silicon
- Crystal properties; native and mechanically induced defects and their characterization
- Gettering and other effects of thermal processing on defects
- The impact of microdefects on MOS and on bipolar devices
- The effect of microdefects on radiation hardening of devices

The talks will be followed by an extensive discussion period involving both a panel of experts and audience participation.

NOTE: Since facilities for this workshop will necessitate a limited attendance, a preliminary level of interest is being solicited to aid in planning. If you feel you would like to attend, please return the form below before December 20, 1975 to:

J. R. Ehrstein
National Bureau of Standards
Building 225, Room B-346
Washington, D. C. 20234

---

I am interested in attending the workshop on Microdefects.

Name: _____

Company: _____

Address: _____

UNITED STATES DEPARTMENT OF
COMMERCE
NEWS
WASHINGTON, D.C. 20230

NATIONAL BUREAU OF STANDARDS
Washington, D.C. 20234

TECHNICAL NEWS from the National Bureau of Standards

Fred McGehan
301/921-2816

FOR IMMEDIATE RELEASE
Mailed: October 28, 1975

TN-4735

## NBS VIDEOTAPE AVAILABLE ON LASER SCANNING OF ACTIVE SEMICONDUCTOR DEVICES

New and powerful applications for laser scanning in semiconductor device design and reliability work are presented in a videotape now available for distribution on loan without charge from the National Bureau of Standards (NBS).

Titled "Laser Scanning of Active Semiconductor Devices," the 55-minute presentation is given by David E. Sawyer and David W. Berning, developers of an optical scanner which can, in a completely nondestructive way, reveal the inner workings of semiconductor devices.

As an added feature, Sawyer and Berning, both of the NBS Electronic Technology Division, are available for a telephone conference call to answer questions and provide more detailed information following a prearranged showing of the videotape. In demonstrating some of the many applications of this scanner and in offering construction details, Sawyer and Berning hope that the semiconductor community will be stimulated to construct and use similar scanner systems.

- more -

In the videotape presentation the design of the scanner is described in detail and many of its applications are displayed and discussed. For example, it is shown that the scanner can (1) map dc and high-frequency gains in transistors, (2) reveal areas of the device operating in a non-linear manner, (3) electronically map temperature in the transistor, and (4) detect the location of hot spots that can develop for certain operating conditions. The vehicle used to show the capabilities of the scanner is a bipolar interdigitated UHF transistor. A dual input NAND gate is used to demonstrate the use of the scanner to determine internal logic states and otherwise observe internal operation of the circuit. To show the ability of the scanner to examine MOS devices without detectable degradation, an MOS shift register is used. The location and progress of internal logic in the register is clearly shown by the scanner. Not only can internal logic be mapped and marginally-operating logic cells detected, but individual logic states can, if desired, be changed by the scanner without affecting other elements.

Mapping is performed by scanning the semiconductor device with low-power CW lasers which locally create electron-hole pairs within the structure. These current carriers can stimulate device behavior by taking the place of signal current-carriers which are supplied by leads fixed to the device.

In contrast to signals applied via the fixed device leads, the optical excitation can be moved over the surface and within the bulk. The response of the structure can be studied on a point-by-point basis by displaying the response on a screen whose x-y sweeps are synchronized with the laser scan.

Persons wishing to borrow the videotape should contact Ms. Elaine C. Cohen, Room B346, Technology Building, National Bureau of Standards, Washington, D.C. 20234. The tape is available in color on 3/4-inch cassettes and in black and white on 1/2-inch reels. An earlier videotape, titled "Defects in PN Junctions and MOS Capacitors Observed Using Thermally Stimulated Current and Capacitance Measurements," is also available on loan without charge.

- 30 -

# NBS TECHNICAL PUBLICATIONS

## PERIODICALS

**JOURNAL OF RESEARCH** reports National Bureau of Standards research and development in physics, mathematics, and chemistry. It is published in two sections, available separately:

**• Physics and Chemistry (Section A)**

Papers of interest primarily to scientists working in these fields. This section covers a broad range of physical and chemical research, with major emphasis on standards of physical measurement, fundamental constants, and properties of matter. Issued six times a year. Annual subscription: Domestic, $17.00; Foreign, $21.25.

**• Mathematical Sciences (Section B)**

Studies and compilations designed mainly for the mathematician and theoretical physicist. Topics in mathematical statistics, theory of experiment design, numerical analysis, theoretical physics and chemistry, logical design and programming of computers and computer systems. Short numerical tables. Issued quarterly. Annual subscription: Domestic, $9.00; Foreign, $11.25.

**DIMENSIONS/NBS (formerly Technical News Bulletin)**—This monthly magazine is published to inform scientists, engineers, businessmen, industry, teachers, students, and consumers of the latest advances in science and technology, with primary emphasis on the work at NBS. The magazine highlights and reviews such issues as energy research, fire protection, building technology, metric conversion, pollution abatement, health and safety, and consumer product performance. In addition, it reports the results of Bureau programs in measurement standards and techniques, properties of matter and materials, engineering standards and services, instrumentation, and automatic data processing.

Annual subscription: Domestic $9.45; Foreign, $11.85.

## NONPERIODICALS

**Monographs**—Major contributions to the technical literature on various subjects related to the Bureau's scientific and technical activities.

**Handbooks**—Recommended codes of engineering and industrial practice (including safety codes) developed in cooperation with interested industries, professional organizations, and regulatory bodies.

**Special Publications**—Include proceedings of conferences sponsored by NBS, NBS annual reports, and other special publications appropriate to this grouping such as wall charts, pocket cards, and bibliographies.

**Applied Mathematics Series**—Mathematical tables, manuals, and studies of special interest to physicists, engineers, chemists, biologists, mathematicians, computer programmers, and others engaged in scientific and technical work.

**National Standard Reference Data Series**—Provides quantitative data on the physical and chemical properties of materials, compiled from the world's literature and critically evaluated. Developed under a world-wide program coordinated by NBS. Program under authority of National Standard Data Act (Public Law 90-396).

NOTE: At present the principal publication outlet for these data is the Journal of Physical and Chemical Reference Data (JPCRD) published quarterly for NBS by the American Chemical Society (ACS) and the American Institute of Physics (AIP). Subscriptions, reprints, and supplements available from ACS, 1155 Sixteenth St. N. W., Wash. D. C. 20056.

**Building Science Series**—Disseminates technical information developed at the Bureau on building materials, components, systems, and whole structures. The series presents research results, test methods, and performance criteria related to the structural and environmental functions and the durability and safety characteristics of building elements and systems.

**Technical Notes**—Studies or reports which are complete in themselves but restrictive in their treatment of a subject. Analogous to monographs but not so comprehensive in scope or definitive in treatment of the subject area. Often serve as a vehicle for final reports of work performed at NBS under the sponsorship of other government agencies.

**Voluntary Product Standards**—Developed under procedures published by the Department of Commerce in Part 10, Title 15, of the Code of Federal Regulations. The purpose of the standards is to establish nationally recognized requirements for products, and to provide all concerned interests with a basis for common understanding of the characteristics of the products. NBS administers this program as a supplement to the activities of the private sector standardizing organizations.

**Federal Information Processing Standards Publications (FIPS PUBS)**—Publications in this series collectively constitute the Federal Information Processing Standards Register. Register serves as the official source of information in the Federal Government regarding standards issued by NBS pursuant to the Federal Property and Administrative Services Act of 1949 as amended, Public Law 89-306 (79 Stat. 1127), and as implemented by Executive Order 11717 (38 FR 12315, dated May 11, 1973) and Part 6 of Title 15 CFR (Code of Federal Regulations).

**Consumer Information Series**—Practical information, based on NBS research and experience, covering areas of interest to the consumer. Easily understandable language and illustrations provide useful background knowledge for shopping in today's technological marketplace.

**NBS Interagency Reports (NBSIR)**—A special series of interim or final reports on work performed by NBS for outside sponsors (both government and non-government). In general, initial distribution is handled by the sponsor; public distribution is by the National Technical Information Service (Springfield, Va. 22161) in paper copy or microfiche form.

---

Order NBS publications (except NBSIR's and Bibliographic Subscription Services) from: Superintendent of Documents, Government Printing Office, Washington, D.C. 20402.

## BIBLIOGRAPHIC SUBSCRIPTION SERVICES

**The following current-awareness and literature-survey bibliographies are issued periodically by the Bureau:**

**Cryogenic Data Center Current Awareness Service**

A literature survey issued biweekly. Annual subscription: Domestic, $20.00; foreign, $25.00.

**Liquefied Natural Gas.** A literature survey issued quarterly. Annual subscription: $20.00.

**Superconducting Devices and Materials.** A literature survey issued quarterly. Annual subscription: $20.00. Send subscription orders and remittances for the preceding bibliographic services to National Technical Information Service, Springfield, Va. 22161.

**Electromagnetic Metrology Current Awareness Service** Issued monthly. Annual subscription: $100.00 (Special rates for multi-subscriptions). Send subscription order and remittance to Electromagnetics Division, National Bureau of Standards, Boulder, Colo. 80302.